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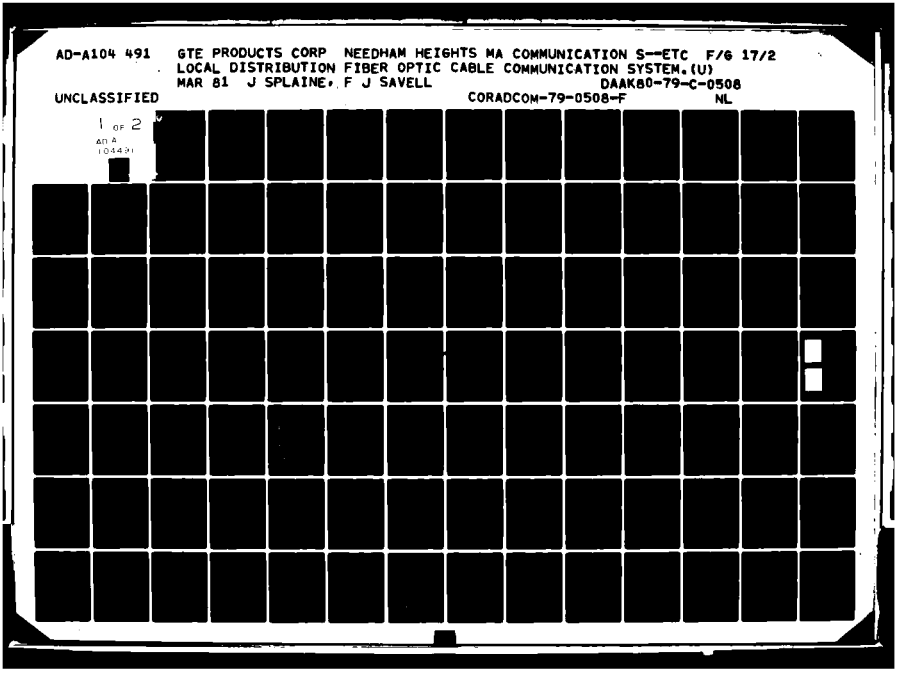

LEVEL II

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RESEARCH AND DEVELOPMENT TECHNICAL REPORT CORADCOM-79-0508-F

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LOCAL DISTRIBUTION FIBER OPTIC CABLE COMMUNICATION SYSTEM FINAL TECHNICAL REPORT

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Communication Systems Division
of the GTE Systems Group
77 A Street, Needham, Massachusetts 02194

5 September 1980

Final Report for Period Feb. 1979 – Sept. 1980

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PREPARED FOR:

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Fiber Optic Communication
AN/TYC-39 Message Switch

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

This report contains the final description of the electrical, electroptical and mechanical design of the fiber optic communication link interconnecting the MS and CI shelters of the message switch (AN/TYC-39). A summary of test results and tests performed at the contractor's facility is provided.

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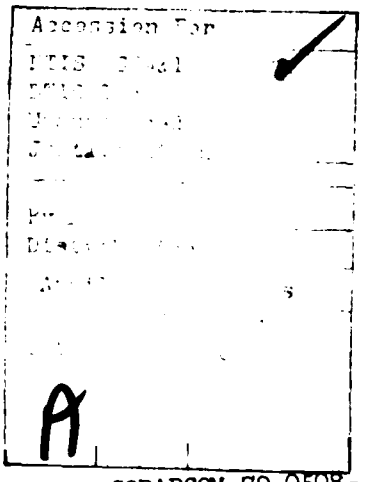

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TABLE OF ABBREVIATIONS

1.	A/D	Analog to Digital
2.	AGC	Automatic Gain Control
3.	BER	Bit Error Rate
4.	CAP	Configuration and Alarm Panel
5.	CI	Communication Interface
6.	CIC	Communication Interface Controller
7.	CICM	Communication Interface Controller Module
8.	CIC-2	Communication Interface Controller
9.	CIP	Communications Interface Processor
10.	CML	Communication Interface Processor/Message Processor Link
11.	CPU	Central Processor Unit
12.	CRSM	Configuration Register and Status Multiplier
13.	C&S	Command and Status
14.	CVSD	Variable Slope Delta Modulator/Demodulator
15.	DGM	Displace Group Modem
16.	DLM	Diphase Loop Modem
17.	DSVT	Digital Secure Voice Telephone
18.	DTG	Digital Transmission Group
19.	EO	Electrical to Optical
20.	ETP	Engineering Test Plan
21.	FIFO	First In - First Out
22.	GB	Group Buffer
23.	GFU	Group Framing Unit
24.	IOX-R	Input/Output Exchange Receiver
25.	IOX-T	Input/Output Exchange Receiver

TABLE OF ABBREVIATIONS (Cont.)

26.	LDCOM	Local Distribution Optical Cable Modems
27.	LED	Light Emitting Diode
28.	LNDR	Line Driver
29.	LTG	Local Timing Generator
30.	M&FI	Maintenance and Fault Isolator
31.	MP	Message Processing
32.	OTP	Operational Test Procedure
33.	OTR	Optical Transmitter/Receiver
34.	PCB	Printed Circuit Board
35.	PWB	Printed Wiring Board
36.	RCHYB	Resistor/Clock Hybrid
37.	TDIC	Time Division Interface Controller
38.	TDIG	Time Division Interface Group
39.	TGM	Transmission Group Modem
40.	TTL	Transistor to Transistor Logic
41.	TTY	Teletype
42.	UART	Universal Asychronous Receiver Transmitter

1.0 INTRODUCTION

From August 1976 through February 1978, GTE Sylvania performed several studies for the U.S. Army Communications R&D Command (CORADCOM) to identify and characterize those areas within the TRITAC network that could benefit most from the application of fiber optic technology. The AN/TYC-39 intershelter cabling systems were selected as best meeting that goal due primarily to the weight, space and resultant life cycle cost savings afforded by the lighter and smaller fiber optic cables. These studies form the basis for the Local Distribution Fiber Optic Cable Communications System (LDFOCCS) program.

1.1 Purpose of LDFOCCS Program

The objective of the Local Distribution Fiber Optic Cable Communications System (LDFOCCS) program is to replace the four 100-foot, double shielded, 26-pair wire cables presently interconnecting the two TYC-39 Message Switch Shelters with a multiplexed fiber optic link. The space and weight savings effected by the replacement of the 26-pair cable with fiber optics makes it possible to eliminate one pallet and associated truck per each pair of message switch shelters. GTE Sylvania has designed the fiber optic transmitters and receivers (optical modems) and has provided the external and internal fiber optic cables/connector assemblies, and has designed the multiplexing and parallel-to-serial conversion hardware to interface with the TYC-39 and convert the parallel digital and analog data into Time Division Multiplexed digital data streams suitable for optical transmission.

1.2 System Overview

Figure 1-1 shows a typical node in the TRITAC tactical communications network. The node contains two major functional elements:

a. A circuit switch for serving analog and digital voice and data subscribers.

b. A message switch for providing store and forward message traffic handling capability.

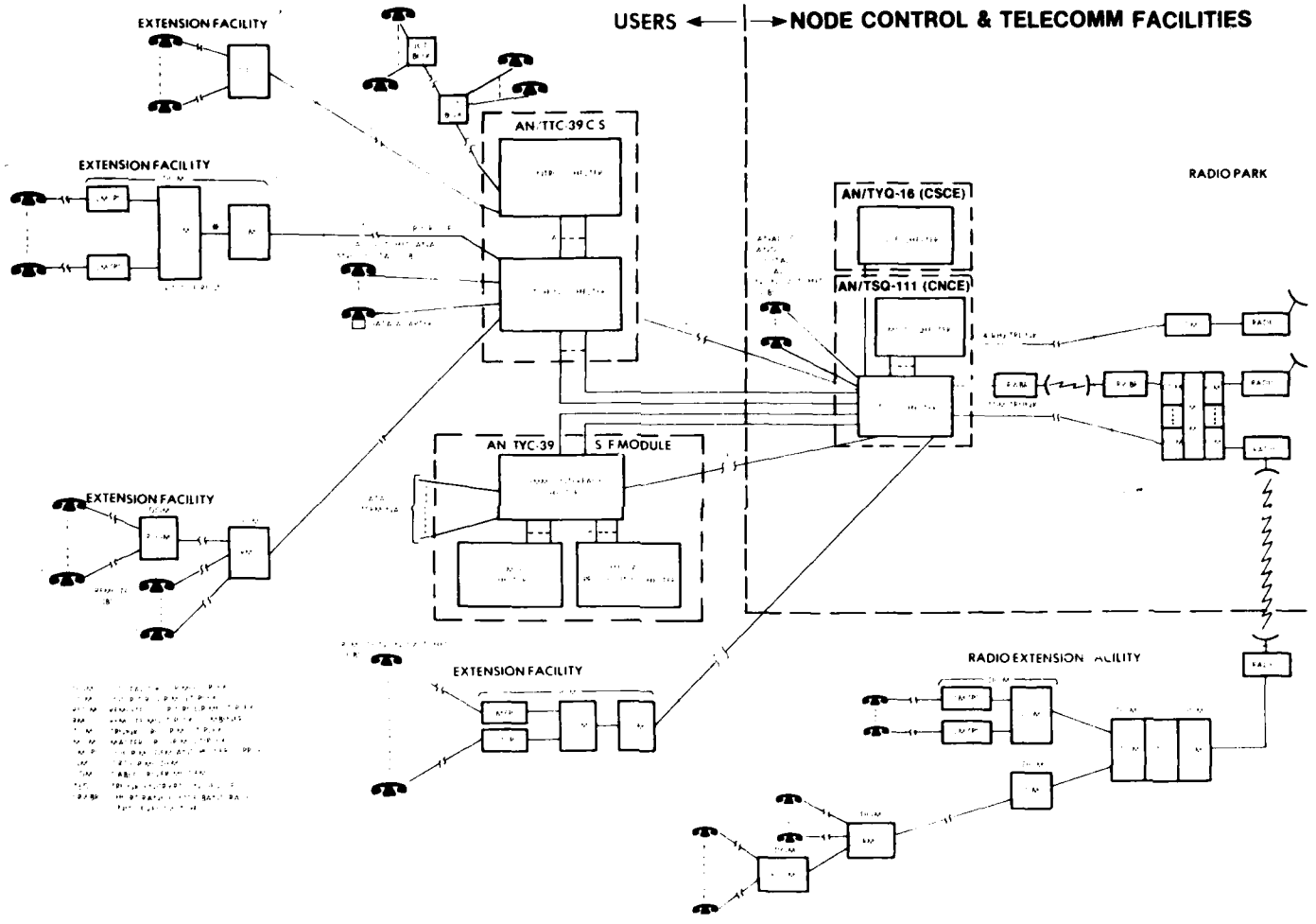


Figure 1-1. Tactical Network Node Communications Elements Connectivity (Illustrative)

The switches are connected to each other, to local and remote subscribers through the Digital Group Multiplex (DGM) equipment, and to other transmission media through the technical control facility. In a typical deployment shown in Figure 1-2, the switches are housed in shelters designed to be transported via truck. The message switch, which is being retrofitted with the fiber optic interconnect system, consists of two shelters, a Communications Interface (CI) shelter which interfaces to outside plant equipment and subscribers, and a Message Processing (MP) shelter which contains switching processors and operator terminals.

Each shelter is supported by pallet-mounted environmental control units and intershelter cabling. Much of the space and volume of each pallet is consumed by the large 26-pair intershelter cable drums, which is the primary motivation for using fiber optics (i.e., to reduce weight, volume, and associated support costs.

1.2.1 Present Message Switch Link Configuration

The present link is implemented with four 100-foot, 26-pair cables which are divided into two functional groupings as shown in Figure 1-3.

a. Two cables carry the command and status group which consist of a variety of analog and digital voice, teletypewriter, and digital command and status signals.
b. The other two cables link a fully redundant control processor set to a communications interface controller which is connected to peripheral devices. (The redundant link is in a hot-standby configuration.)

1.2.2 LDFOCCS Configuration

The existing intershelter link, composed of four 26-pair cables, is replaced by two 6-fiber cable links; as shown in Figure 1-4, three fibers are implemented for each of the two redundant processor I/O channels, three fibers are implemented for each of the two redundant Command/Status channels,

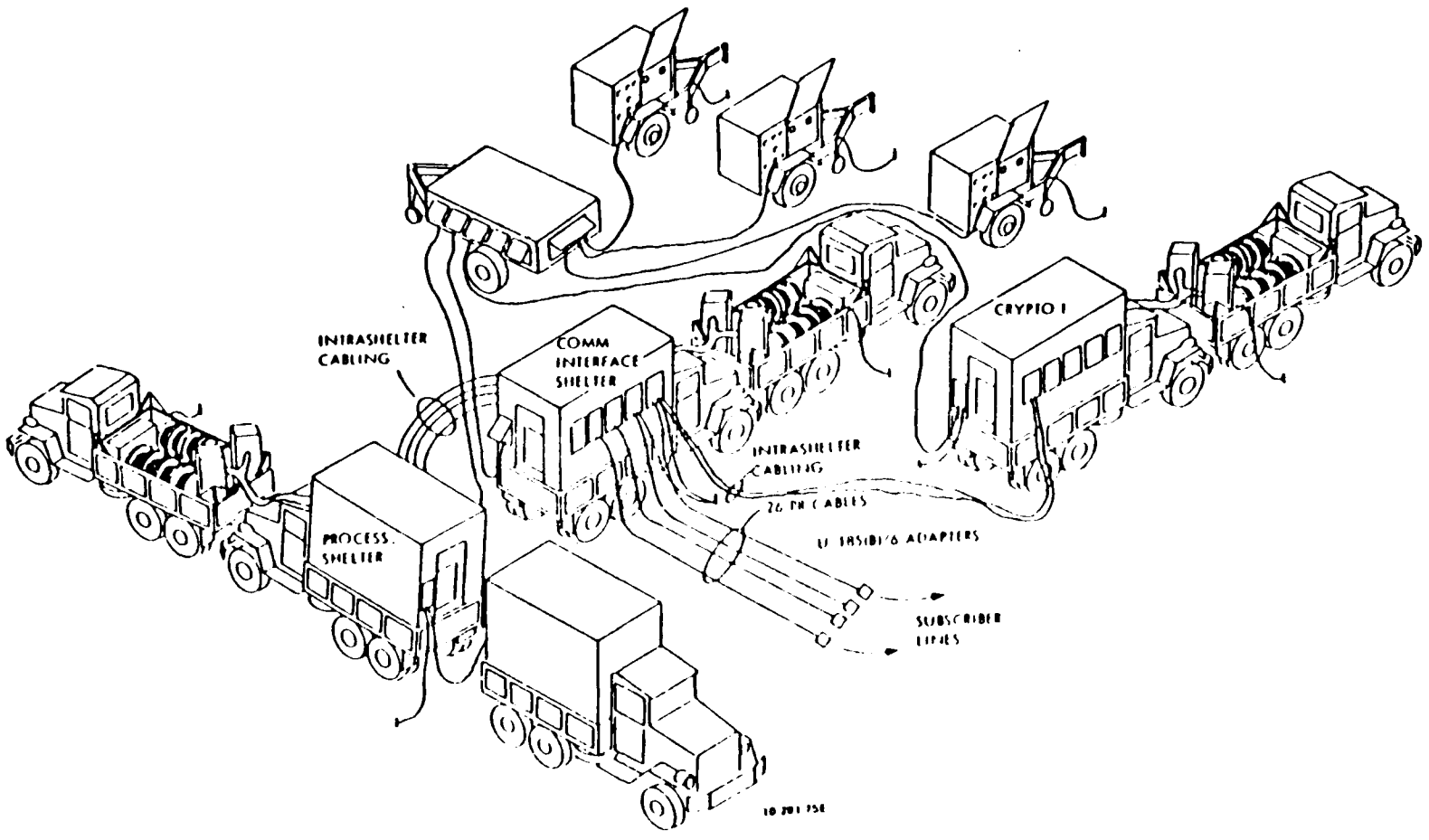


Figure 1-2. Typical Deployment

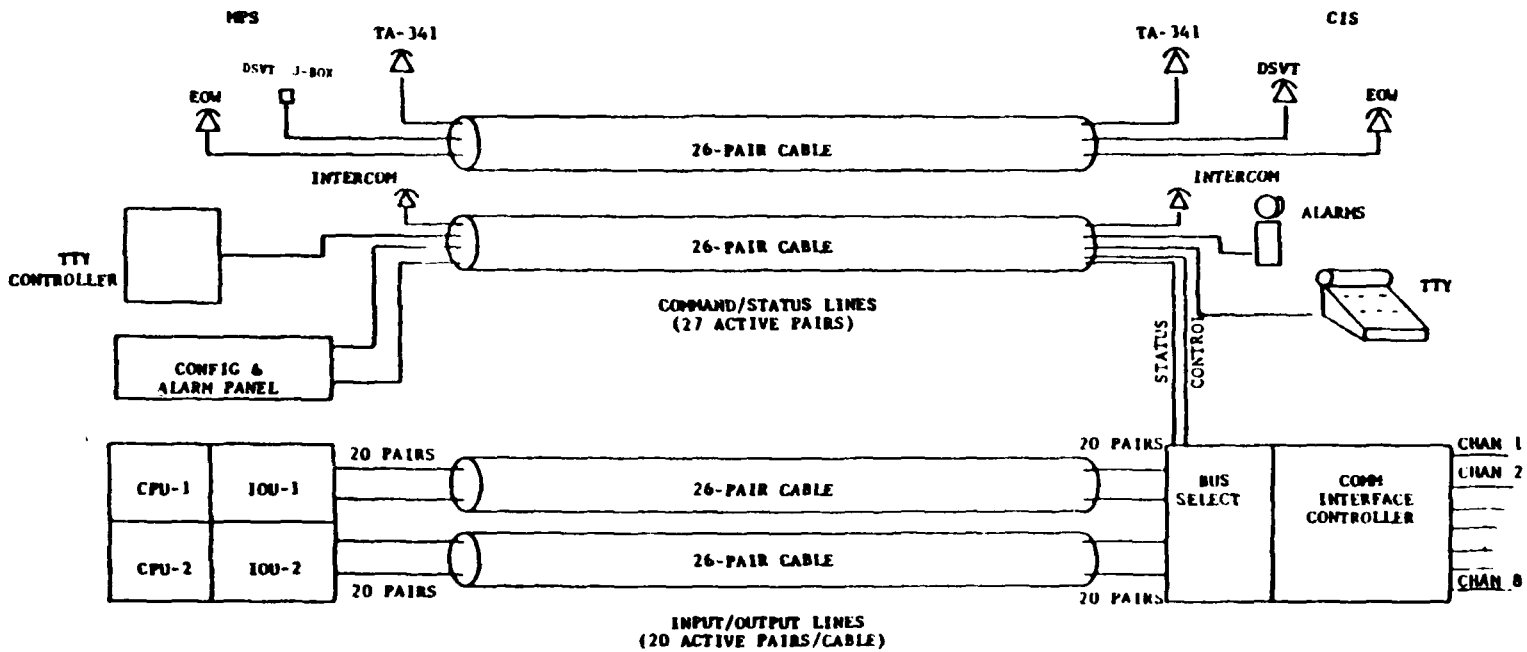


Figure 1-3. Message Switch Intershelter Link Configuration

MESSAGE SWITCH INTERSHELTER LINK – FIBER OPTIC IMPLEMENTATION

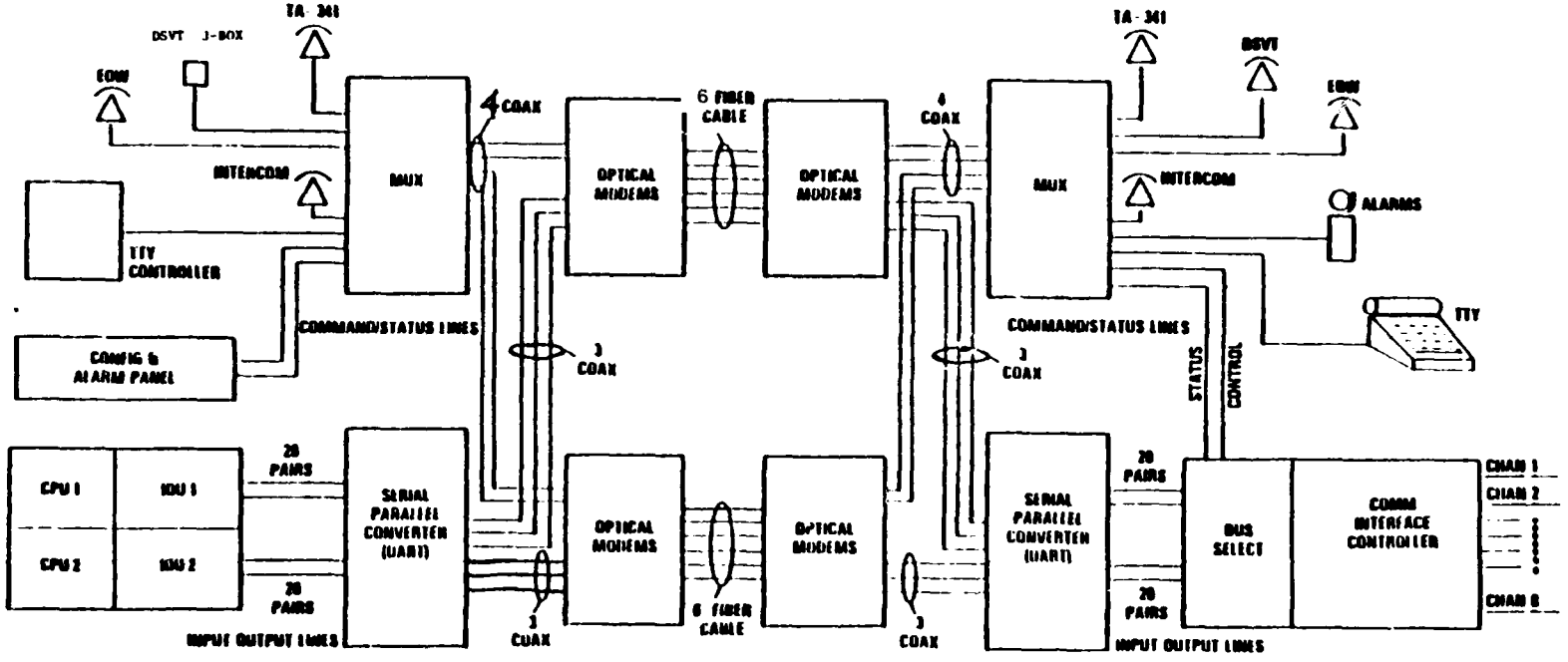


Figure 1-4. Fiber Optic Link Configuration

The optical cable links consist of external cables interconnecting the two shelters and internal cables connecting each shelter's Signal Entry Panel (SEP) at the shelter wall, to its respective card nest. Within the MP shelter, the equipment is housed in a nest containing 20 cards of MUX/Converter logic and two cards of optical modems and the CI shelter contains a nest with 22 cards of MUX/Converter logic and two cards of optical modems interfacing with the Message Switch at selected electrical connectors. The modems interface with one another via multi-fiber connectors at both the card nest and shelter wall interfaces.

1.2.2.1 Command and Status Link Implementation

Figure 1-5 shows the block diagram for the fiber optic implementation of the command and status link. At the transmitting end, analog channels are A/D encoded, multiplexed with digital signals, framed, diphase-modulated to provide timing, and transmitted optically on one fiber by the LED. The composite signal is then converted back to the electrical domain by the PIN photodetector, where the reverse process takes place to recover the individual channels. The result is that two 26-pair cables are reduced to two six element fiber cables.

1.2.2.2 Processor I/O Link Implementation

Figure 1-6 shows the parallel data transfer format between the processor and peripherals. Data is exchanged via nine bi-directional INFORMATION lines under control of the processor COMMAND AND ENABLE lines. A key requirement that influenced the design was that the peripherals acknowledge with an INDICATOR signal 1500 ns after receipt of a processor command. Because of this timing requirement, the Processor I/O fiber optic implementation uses three fibers for each redundant link; one fiber is dedicated to the INDICATOR signal, while the other two fibers provide full-duplex data exchange (Figure 1-7). The operation of the two data exchange fibers is similar to a Universal Asynchronous Receiver Transmitter (UART) in that the parallel data is buffered and converted to serial format and then transferred asynchronously with START/STOP bit control.

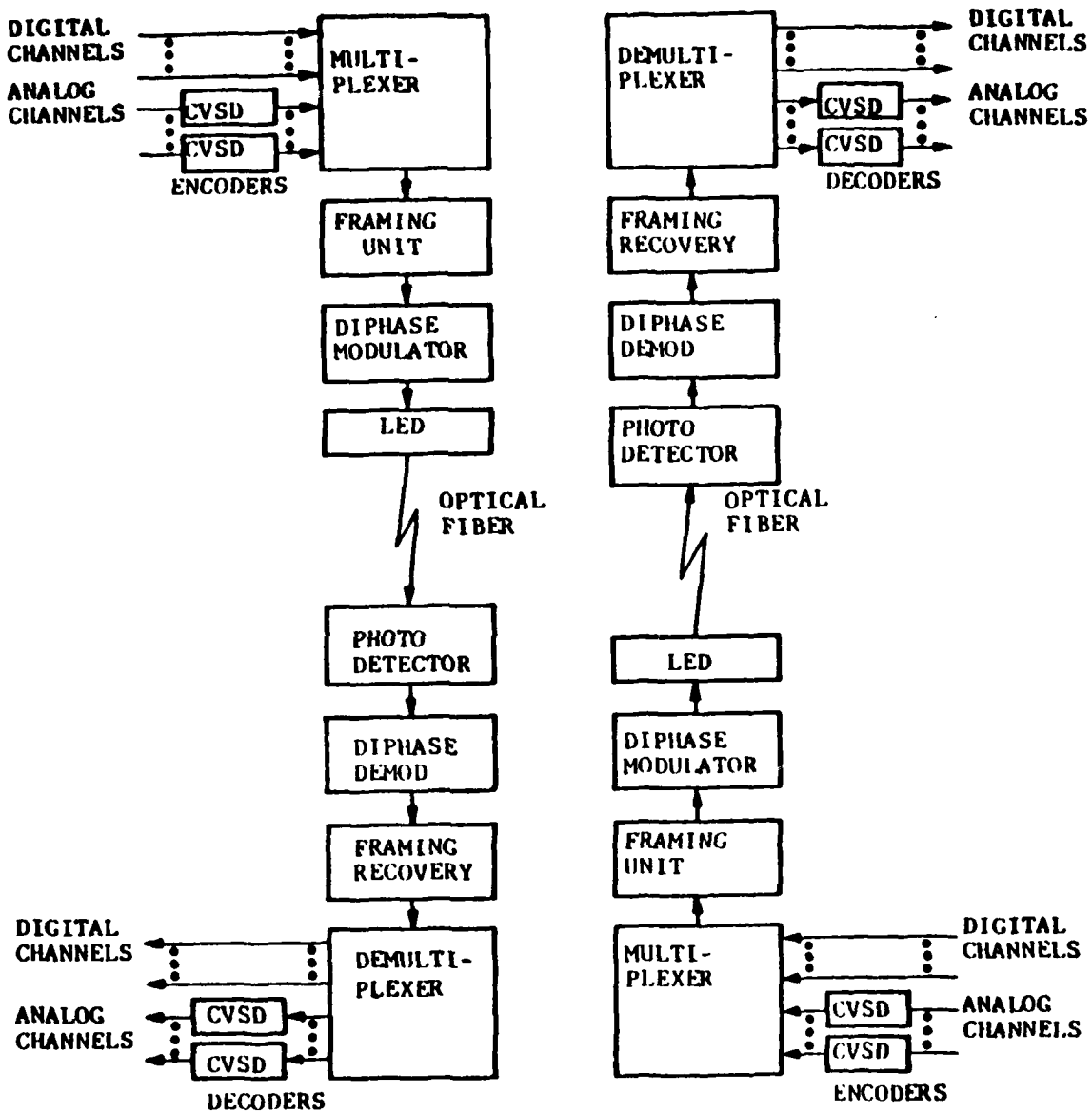


Figure 1-5. Command/Status Fiber Optic Link Block Diagram

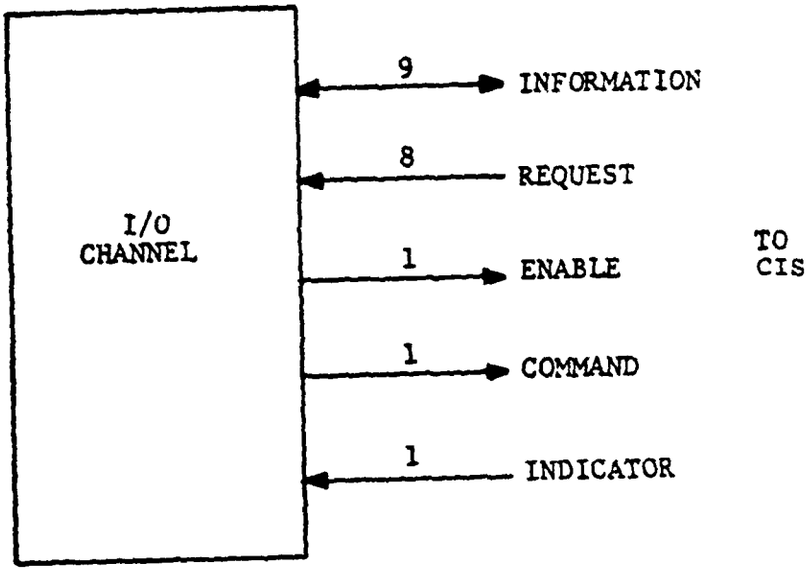


Figure 1-6. Input/Output Lines Data Format

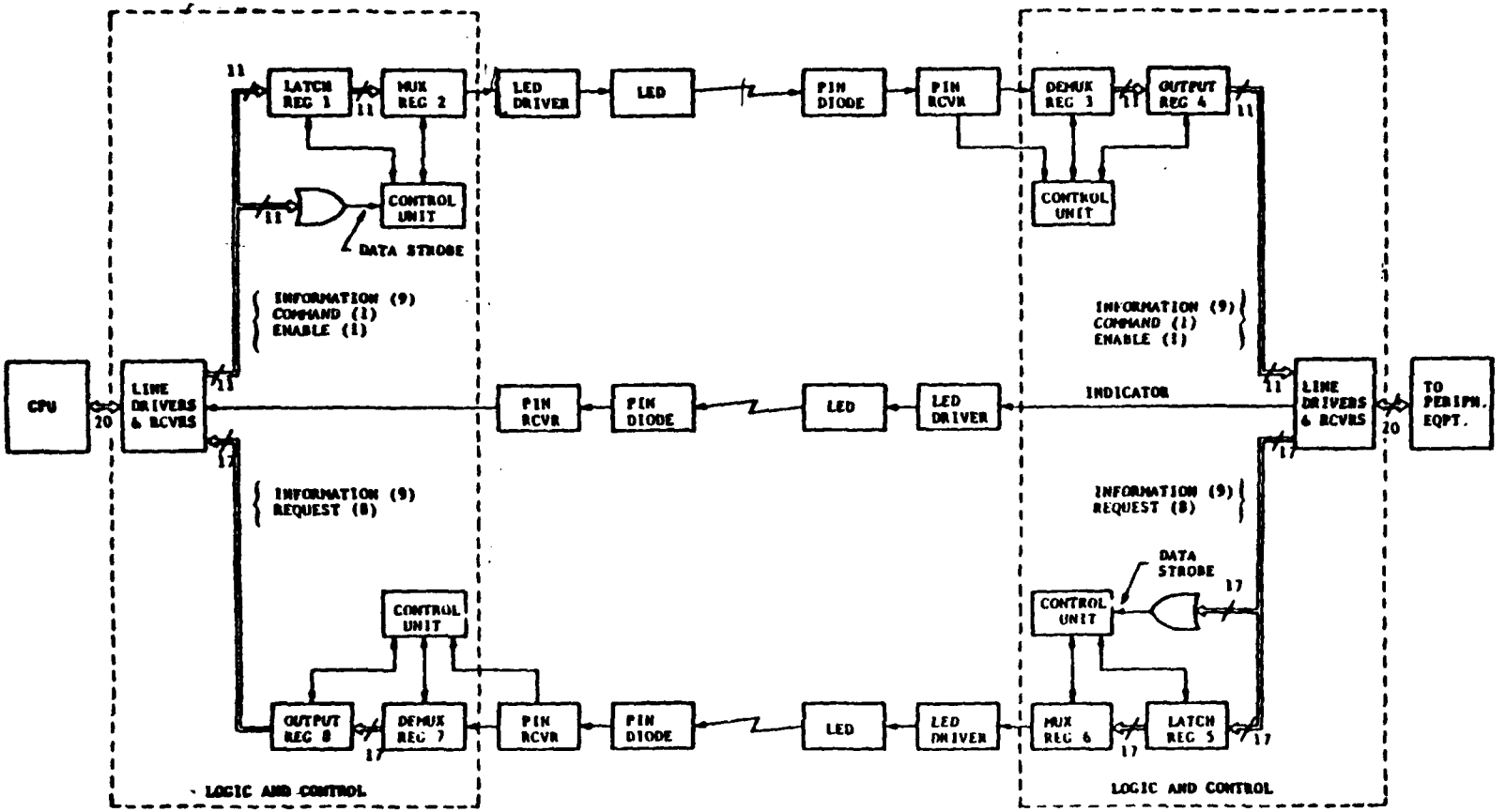


Figure 1-7. Input/Output Channel Fiber Optic Link Block Diagram

2.0 SUMMARY

2.1 LDFOCCS Major Task Summary

In order to meet the objectives of this program, a Local Distribution Fiber Optic Cable Communications System was designed to provide interconnection of the processor input/output lines (two redundant processors are utilized) and communications and status lines between the Communications Interface Shelter and Message Processing Shelter of the AN/TYC-39 Store and Forward Module (Message Switch). This system replaces the four 26-pair cables presently utilized for this purpose. The system consists of the following:

a. Two Local Distribution Optical Cable Modems (LDOCM) (one each shelter).

b. Two ruggedized fiber optic cable assemblies.

The design effort included:

- Subsystem design and performance analysis
- Optical component trade-off studies and selection
- Physical accommodation study and design
- Detailed electrical and mechanical design of the LDOCM hardware
- Build and test of engineering breadboards of the I/O link parallel-to-serial converter and the optical transmission subsystem.

2.1.1 LDOCM

The LDOCM hardware comprises the following equipment groups:

- Parallel-to-serial (PS) Converters
- E-O Converter Assembly
- E-O Converter-to-SEP Optical cable assembly.

The PS Converter incorporates the hardware necessary to time division multiplex the parallel analog and digital inputs into serial output data streams for transmission over fiber cables, including A/D-D/A conversion. MUX/DEMUX, synchronization, and data modulation. The E-O converter assembly includes Fiber Optic Cable Drivers, Fiber Optic Cable Receivers,

6-channel Bulkhead Fiber Optic connectors, and six-channel card-edge fiber optic connectors.

2.1.2 Ruggedized Fiber Optic Cable Assemblies

The system utilizes two ruggedized six-element fiber optic cable assemblies. Each cable assembly dedicates three fibers to one of the redundant IOX links, and three fibers to the C&S link. This will provide for two fully operationally redundant IOX links and pluggable standby redundancy for the C&S links.

2.1.3 Production

One complete Local Distribution Fiber Optic Cable Communications System kit was fabricated together with two spare Fiber Optic Cable Assemblies, and one set of replacement printed wiring boards providing one spare of each different circuit card type used in the system.

2.1.4 Test Program

As part of the program, the following test-related tasks were performed.

2.1.4.1 Optical Component Performance Verification Test

Laboratory testing of all received optical components (LEDs, optical cables, connectors, detectors) were performed to ensure that they met critical manufacturer's specified performance parameters prior to incorporation into the system. Parameters verified include LED power output, connector insertion loss, fiber attentuation, and detector sensitivity.

2.1.4.2 Acceptance Test Program

GTE Sylvania conducted an acceptance test program of the LDFOCCS equipment to demonstrate compliance with the requirements of section 3 of the LDFOCCS system specification, EL-SS-0198-001A, 7 March 1978. This program included the individual tests, analyses, and inspections listed below.

1. Operating and nonoperating environmental tests, performed at GTE Sylvania's Needham facility, in accordance with Section 4.3 of the specification. Tasks associated with this test included preparation of test plans and procedures (subject to Government approval), test performance, and preparation of a test report.

   The following category of tests were performed on the PC cards:

   a) Fungus
   b) High Temperature
   c) Low Temperature

   The PC cards tested were the IOX-T, IOX-R, OTR and RCHYB. Since the PC cards were not configured as final production prototype models the following tests were waived: Humidity, Vibration, Shock and Bench Handling.

   The following test was performed on the optic cable/ reel assembly and transit case:

   a) Vibration (Loose Cargo)

2. Mechanical and visual inspection in accordance with Section 4.6 of the specification.

3. System safety engineering inspection in accordance with Section 4.8 of the specification.

4. Reliability analysis in accordance with Section 4.4 of the specification.

5. System level performance tests at Needham using the MS #7 in accordancewith Section 4.5 of the specification. Tasks associated with this test included preparation of test plans and procedures (subject to Government approval), test performance, and preparation of a test report.

The acceptance test program applied only to those printed wiring board or assembly types that had not undergone prior Government-approved acceptance testing. The Government waived acceptance test requirements for printed wiring board or assembly types that had previously undergone a Government-approved acceptance test.

2.2 Results

2.2.1 System Integration and Test

2.2.1.1 Description

The LDFOCCS equipments were installed in the AN/TYC-39 Message Switch system #7, serial #5. The Message Switch consists of (2) S280 shelters, a message processing shelter and a communication interface shelter. The LDFOCCS equipments consist of (2) nests, one in each shelter, each containing the necessary logic. It also consists of the interconnecting fiber optic cables. The software used during the system integration and test phase consisted of the following:

1. Simple machine language programs entered into the system via the VDU. The reason for using these programs is that they provide a controlled environment so that the critical timing can be checked.

2. Exerciser Programs. These are existing programs that are used for hardware checkout of the TYC-39 equipments. These programs exercise the hardware more thoroughly than the simple programs in 1 above.

3. Maintenance and Fault Isolation (M&FI) Programs. These programs are similar in complexity to the exerciser programs above. These are run for two reasons. One is that they provide a higher level of confidence that the equipment is operating. The other is that the TDIG M&FI program is part of the sell-off procedure.

4. Operational Programs. These are the programs that are used for Message Switch operation.

The testing phase proceeded as follows; The LDFOCCS equipments can be broken up into three functional areas, command and status link, I/O link, and optics. The philosophy of testing therefore was to test each individual area independently, correcting any problems that occurred, and then integrating all three together.

2.2.1.2 Problems Identified and Solutions Implemented

A. Command and Status (C&S) Link

The major problem encountered with the C&S link was synchronization. The MP to CI link could intermittently fall out of sync with one another. Two problems were encountered. One was that the 16 MHz clock was noisy. This was corrected by using differential drivers and receivers when running the clock down the nest. Another problem was that the 32 MHz clock was unstable. This was corrected by using a more stable source.

B. I/O Link

Three major problems were encountered when integrating the link. One was a contention I/O problem where request information arriving at the remote end of the link was chopping off a data byte to the computer, thus causing the computer to time out. This was fixed by insuring that data transfer take priority over requests. Another problem was transmitting the indicator signal as part of the data word. This was also causing contention problems. This was corrected by sending all indicators over a separate fiber. The last major problem was that there were intermittent device timeouts and level 2 errors being reported by the processor. A timing error was found in the transmit inhibit logic and was corrected.

C. Optics

Two major problems occurred on the optical transmitter/receiver, OTR, circuitry. One was the poor operation of the Automatic Gain Control (AGC), circuitry. It could not respond fast enough and was consequently stretching the pulses. This circuitry was eliminated and replaced by a hard limiting circuit. The other major problem was that extensive jitter was occurring on the data signals. This was compensated for by putting potentiometers on the comparator portion of the receivers so that the threshold of the circuit could be tuned. The threshold had a direct relationship with the pulse width consequently the jitter could be centered for optimum performance.

D. Other Problems

1. DSVT would not work in either direction. It was discovered through discussion of DSVT operation that it was not going to operate as the logic was implemented. In order to correct the problem a redesign making the diphase loop modem in the MP shelter a slave would have to be incorporated. Since time was at a premium and since it was estimated this would take two weeks the problem was not corrected. This problem does not occur in the Phase II LDFOCCS because a separate cable is being used for communication.

2. TDIG M&FI program would not operate properly. Although the TDIG operated properly during the Group A test the M&FI program gave a false error indication when run. Again because of the time limitations the problem was not solved.

D. Other Problems (Cont.)

3. One rollback on CICM and CRSM when configuring. Each time the CICM or CRSM was reconfigured a ROLLBACK printout, indicating the configuring was unsuccessful, would occur. We suspect this problem was due to the extra delay added to the status lines coming from these devices but again there was no time to solve this problem.

2.2.1.3 Product Improvements

A. Optics

The Optical Transmitter/Receiver printed circuit card was redesigned for the Phase II LDFOCCS program with the following improvements. The design was simplified with fewer components for better performance. The AGC circuitry was eliminated. The detector amplifier module was replaced with a simpler detector. The bandwidth of the pulse detector amplifier was increased to handle faster rise and fall times. DC coupling was used to reduce a pulse width dependency on duty cycle and pulse amplitude.

B. Command and Status Link

The C&S link was redesigned eliminating the nonredundant analog implementation and replacing it with a completely redundant digital approach.

C. Others

Other product improvements include a redesign of the IOX-R card making it less pulse width sensitive and the addition of a processor interface cards so that status information of the LDFOCCS logic is available to the software.

2.2.2 Functional Acceptance Test (Group A) Results

The functional acceptance tests of the LDFOCCS Advanced Development Model equipment began on 25 August 1980 and were completed on 28 August 1980. Except for the problems stated above the equipment passed.

2.2.3 Environmental Acceptance Test Summary

2.2.3.1 General

Elements of the Local Distribution Fiber Optic Cable Communication System (LDFOCCS) were environmentally tested during the time period of June 27 through September 2, 1980 according to the applicable sections of the Environmental Test Plan (ETP) given in CDRL F001, Engineering Design Test Plan (7 May 1980). As a schedule expedient for the LDFOCCS subsystem in operational test window at Ft. Huachuca a meaningful subset of tests were conducted according to the ETP.

Fungus
(on selected components)

High Temperature
(on IOX Subsystem cards)

Low Temperature
(on IOX Subsystem cards)

Loose Cargo Bounce
(Fiber-Optic Cable/Reel/
Transit Case)

2.2.3.2 Fungus Test

Equipment Under Test

Samples submitted for the Fungus Test were those recommended in the Test Plan with the approval of the procuring agency:

4 items, Optical Fiber terminated with *single pin contact*
ITT Cable, GTE PN-06-1344005-1
Hughs Contact, PN-1093202-052S/100

1 item, Oscillator Module, Erie Frequency Control PN-20AC1471-(100 mhz)

1 item, Optical Receiver, RCA PN-7946C-30951E

1 item, Optical Transmitter, Laser Diode Labs PN-13-511923-2

Purpose

The purpose of the test was to verify that the devices would provide no nutrients in material, coating, or contaminant form or support fungal growth, as required by EL-SS-0198-001A Local Distribution Fiber System Cable Spec. (7 March 1978) section 3.4.6.1.6 tested per section 4.3.1.6 using MIL-STD-810C Method 508.1, Procedure I.

Results and Conclusions

The test was conducted during the time period of June 27 through July 25, 1980 at Sanders Associates, Nashua, NH.

All four types of test samples were fungus resistant to the five cultures specified by the procedure.

2.2.3.3 Loose Cargo Bounce Test

Equipment Tested

The assemblies under test were the Optical Cable assembly GTE PN-09-1344001-2 mounted on a transport reel GTE PN-82-1362257-1 and housed in a transit case Thermodyne PN-1212-05-05. Pre and post electro-optical tests were conducted per Operational Test Procedure For Fiber Optic Cable Assembly.

Purpose

The purpose of the test was to show that the fiber-optic cable assemblies are capable of withstanding the vibration and shock induced during vehicular transportation per the requirements of EL-SS-0198-001A section 3.4.6.2.9 and tested per section 4.3.2.8.2. The testing section requires the use of MIL-STD-810C, Method 514.2, Procedure XI, Part 2.

Results and Conclusions

The test was conducted at Associated Testing Laboratories in Burlington, Mass. on August 27, 1980. Visual examination of reel, cable, and transport case revealed no discrepancies other than some unevenness in the foam insert in the case. Optical loss measurements per the procedure were taken before and after bounce with insignificant differences noted when measured across the 6 fibers. Post visual inspection noted that the foam padding had been partially cut by the reel and some of the connector cover screws on the Hughes connectors had been vibrated out, dropping into the case. In short, the cable assembly functionally survived the test and the reel/case combination had done their job of protecting the cable assembly during the simulated transportation.

2.2.3.4 High/Low Temperature Tests

Equipment Tested

The assemblies under test during the environmental test phase of LDFOCCS I which required PCB operational test verification were those designs new to the AN/TTC-39 collection of PCBs namely:

IOX-T	PN-06-1360907	SN-1006 B/C & SN-1007 B/C
IOX-R	PN-06-1360908	SN-1005 C/E SN-1007 C/E
OTR	PN-06-1360883	SN-1001 F/F
RCHYB	PN-06-1360887	SN-1006 A/D

The above assemblies were mounted on a UUT-Chassis wired to emulate a typical configuration of an IOX-Link as it would be used in the Message Switch. The UUT-Chassis was operated by the IOX tester using the Operational Test Procedure (OTP) 00-1363487 (Appendix 1.0). For a description of IOX Tester and UUT-Chassis see Appendix 2.0.

Purpose

The purpose of the High and Low Temperature Test was to verify performance of those subassemblies new to the AN/TTC-39 Message Switch per section 3.4.6.1.2 & 3.4.6.1.3 Environmental Requirements of specification EL-SS-0198-001A (7 March 1978) at operating (51.6^{o}C to -25F) and storage temperatures (+62^{o}C to -56.2^{o}C).

Results and Conclusions

The tests were conducted at the environmental test facilities of GTE Sylvania, Bldg 5, Needham Heights, Mass. during the time period of August 25 through September 2, 1980.

Baseline pre-high temperature test results both in terms of functional performance (OTP) and bit-error (BER) tests met the specified electrical/functional criteria of the subsystem specification. However, at elevated operating temperature even though the OTP operated correctly, the BER Test accumulated 70 bit-errors in 4 hours and therefore did not meet the criteria of not more than 3 bit-errors in 4 hours.

The BER Test at elevated temperature pointed out the shortcomings of the Optical Receiver circuit original design, which, due to its capacitively coupled fixed-gain stages would produce narrowing or widening of bit pulses as a function of temperature. These effects will be effectively removed in the new design of the OTR card with the use of a DC-coupled limiter which is DC-coupled to the comparator.

Post-high/pre-low temperature OTP operated satisfactorily other than some instability noted in Step 6 of the OTP (Frame-sync loss). The BER test however, would not run any length of time without high error counts (counter overflow). Optical receiver pulse widths were checked and adjusted for optimum performance. However, when the OTP was initiated at -32°C no pulses were being received in either optical-link direction at the receiver outputs. Catastrophic failure had occured. These failures appeared to be in the Laser Diode Labs LED. Previous problems with these devices falling apart during handling and under soldering temperatures had been experienced during the PCB assembly process. This was due to the quality or type of epoxy and the deficient quantity of epoxy holding the fiber lead in alignment with the LED. It is believed that the devices that made it through the assembly process ultimately failed when subjected to -32°C temperatures. The drive signals were present at the inputs to the LEDs but there was no observable light output from the fiber optic lead end.

Recently received samples of redesigned devices have a plastic coating/shroud which hold the fiber in alignment with the LED and should correct this problem.

3.0 DESIGN DESCRIPTION

3.1 IOX Link Electrical Design

3.1.1 Parallel/Serial Converter

The design of the P/S Converter within the IOX Link Subsystem appears transparent to the I/O communication process taking place between the Litton L3050 processor in the MP shelter and the peripheral devices in the CI shelter. The communication process takes place via the ac coupled IOX bus because the dc bus is internal to the processor and inaccessible. With the insertion of the fiber optics nest at the present wire-line interface at the shelter SEP, dc restoration must take place via the CIC-2 printed circuit board, which will provide the TTL interface before multiplexing the I/O lines to a single-bit stream. Design implementation of the new IOX card (two at each end of link, for each 6-fiber cable) is accomplished using a variety of 54S, 54LS, and ECL logic families.

Before describing the subsections of PS conversion, it is necessary to understand the general nature of the I/O communication process and the nature of the peripheral devices. (Devices will not be described in detail here as they are covered in voluminous specification documents). The nature of the I/O process is summarized here in the form of I/O Instruction Set in Table 3-1. In the table, each instruction is defined, along with the sequence of characters passed and the origination of the character.

The processor is the Litton L3050, which can generate and receive all information defined in Table 3-1. The peripherals in the CI shelter, briefly, are the CML and TDIG. The CML (CIP Message Processor Link) can be thought of as a computer/computer interface buffer. It transacts the passage of memory and status bytes between a Delco computer associated with the CIC rack in the CI shelter and the Litton L3050 computer in the MP shelter.

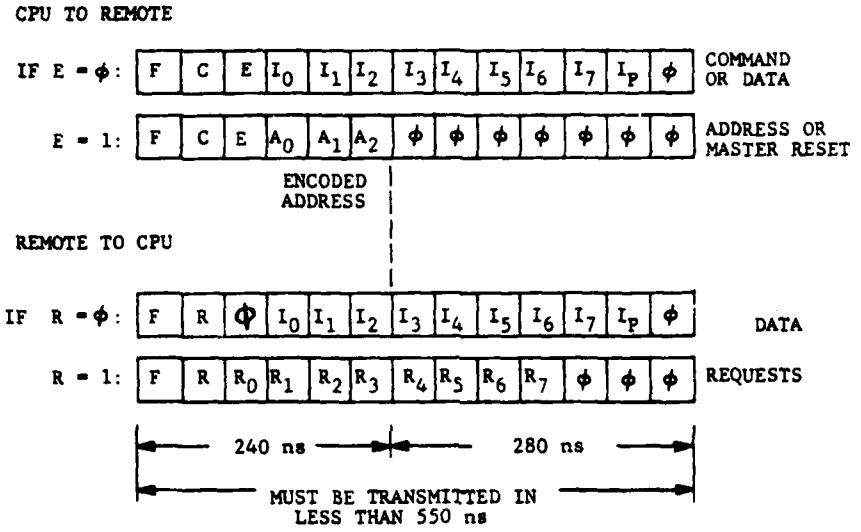
TABLE 3-1 I/O INSTRUCTION SET

I/O Instruction	Sequence of Events	Event Name	From	Comments
DEV	1. C & one I_n address bit	Command	MP	Device Instruction
	2. I_0, I_3= DEV	Instr.Opcode	MP	places device into
	3. I_n=device control byte	Control data	MP	control state or
	4. I-bit	Acknowledge	CI	program load state.
OFR	1. C & one I_n address bit	Command	MP	Output From Register
	2. I_0, I_4= OFR	Instr.Opcode	MP	one memory word is
	3. I_n= 1st Data byte	Data	MP	transferred from
	4. I_n= 2nd Data byte	Data	MP	MP to CI
	5. I_n= 3rd Data byte	Data	MP	
	6. I_n= 4th Data byte	Data	MP	
	7. I-bit	Acknowledge	CI	
ITR	1. C & one I_n address bit	Command	MP	Input To Register
	2. I_0, I_5 = ITR	Instr.Opcode	MP	one memory word is
	3. I_n= 1st Data byte	Data	CI	transferred from
	4. I_n= 2nd Data byte	Data	CI	CI to MP
	5. I_n= 3rd Data byte	Data	CI	
	6. I_n= 4th Data byte & I-bit	Data/Ack	CI	
AI	1. R_n	Request	CI	Automatic Input
	2. E & one I_n address bit	Go Ahead	MP	requires L3050 to
	3. one to four I_n Data bytes	Data	CI	prep term.word & DEV
Alarm	1. R_n	Request	CI	Event Counting
	2. E & one I_n address bit	Go Ahead	MP	Interrupt optional
	3. I-bit	Early Interrupt	CI	at device discretion.
AO	Same as AI but data from MP			Automatic Output
EOB	1. C & one I_n address bit	Command	MP	End of Block
	2. I_0, I_6= EOB	Instr.Opcode	MP	Computer thinks
	May lead to DIO			device finished.
DIO	3. Rn	Request	CI	Device Interrupt Opn
	4. E & one I_n address bit	Go Ahead	MP	Optional, device
	5. I-bit		CI	status summary.
	or I_n=data byte & I-bit	Status byte	CI	
DSO	1. C & one I_n address bit	Command	MP	Device Stop Opn
	2. I_0, I_7 = DSO	Instr.Opcode	MP	Places device in
	3. Device to standby		CI	standby condition.
MR	1. C & E	Command	MP	Master Reset all devices to standby

There are three address channels assigned to each CML, one for transmitting data, one for receiving data, and one for status. The CML has only one group of three channels on-line at a time. The TDIG (Time Division Interface Group) is responsible for conversion of the interface with the Digital Transmission Group (DTG) to individual full duplex channels. The recovered channels are routed to the Communications Equipment Support Group (CESG) where they are patched to TENLEY Loop Key Generators (LKGs) if encrypted, or CIG if unencrypted. TDIG recovers an overhead channel from the trunk group containing framing, signaling, and SYSCON subchannels. The signaling and SYSCON subchannels are transmitted to the MPS. The Time Division Interface Controller (TDIC) is the peripheral device that directly interfaces with the Litton L3050 Processor via the IOX link. One device address is for TDIC TRANSMIT and one for RECEIVE. TDIC provides for a one-word buffer for the RECEIVE channel and one for the TRANSMIT channel, and is responsible for reporting status from the TDIG fault and status register via Status Interrupt and Status Byte or Word.

Since both the CML and TDIC devices utilize most of the Instruction Modes listed in Table 3-1, the entire set then is considered to be required to pass over the IOX link.

The IOX multiplexing converts COMMAND, ENABLE and nine Information lines in parallel to a single data bit stream. Parallel bits, although arriving at the MP next in bursts, can have a 1.818-megabit rate (maximum). In the reverse direction, the single bit stream must be demultiplexed and applied in parallel to the Indicator Line and nine Information lines or to eight Request lines. From the CI nest view, the above processes takes place in reverse order. The data format for the serial transmission has been chosen to be that shown in Figure 3-1. Note that the UART format of adding a start bit (F) and a stop bit (0) to the 11-bit maximum length word adds up to a 13-bit transmitted burst at a minimum of 23.64-megabit rate. A 25-megabit rate is chosen for the IOX link, making each data bit period 40 nanoseconds.



$\frac{13 \text{ BITS}}{550 \text{ ns}}$ = 23.64 MB/s MINIMUM

∴ 25 MB/s IS USED MAKING EACH PIT PERIOD 40 ns AND 13 BITS ARE TRANSMITTED IN 520 ns.

THE ADDRESS TRANSMISSION TAKES 6 BIT PERIODS OR 240 ns.

Figure 3-1 Data Format

The data formats being used in the IOX Link are shown in Figure 3-1. From CPU to REMOTE, the stream beginning is marked with a logic ONE as a framing bit. The COMMAND and ENABLE bits follow, and are first in the transmission to allow for the link logic to know the form of transmission format. (That is, whether a group of I_n or A_n bits are to follow). If the E-bit is a ZERO, the Information lines are placed as is into the bit stream. If E-bit is a ONE, the Information lines which contain an address in the form of one-of-eight code are encoded to a three-bit binary number, which are positioned in the next three time slots. This makes the address available within 240 nanoseconds of the beginning of the transmission to aid in speeding up I-bit round-trip delay during Alarm mode, or Status Interrupt operations. The last bit position is a dedicated ZERO as a stop bit.

From REMOTE to CPU, the transmission length is the same with framing and stop bits used. The R-bit as a ZERO denotes that the transmission is Data.
The R-bit as a ONE denotes that the transmission is Requests.

There can be several request bits transmitted in the same transmission, because requests from devices may be held back while other types of transmissions are already in progress.

3.1.1.1 Subsystem Description

The four basic functional elements of the IOX parallel-to-serial conversion are shown in Figures 3-2 through 3-10, along with their respective control flows.

3.1.1.1.1 CPU Transmitter (MPS Nest)

The CPU transmitter contains an input data storage register which accepts Command, Enable, and Information bits 0-P. The outputs of this 11-bit register are presented to MUX logic, a collection of AND-OR Select gates that allow direct transfer into the Shift Register of the C, E and I_o,I_p bits when address encoding is not required, or 3-bit ADDRESS ENCODE plus dummy ZEROs when address encoding is required. Logic outputs from the Control Unit present LOAD level, CLEAR level, or output shift CLOCK at the appropriate times according to the control

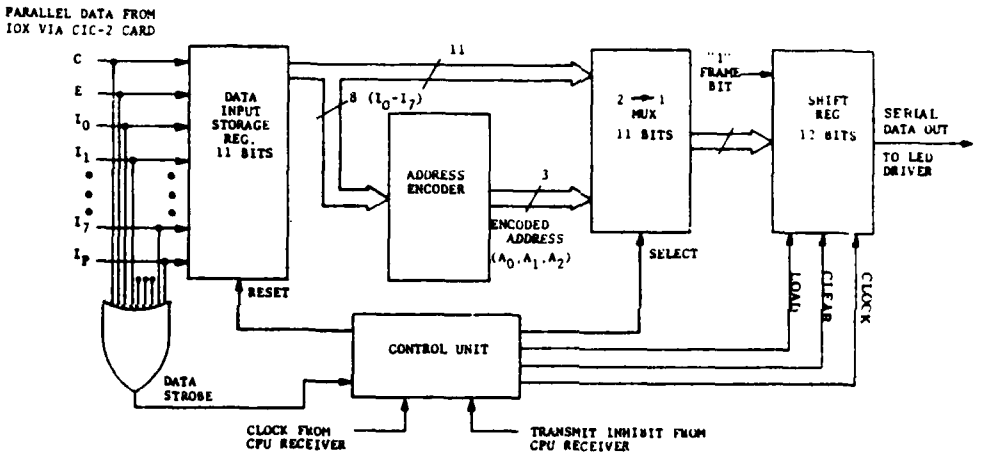


Figure 3-2. CPU Transmitter

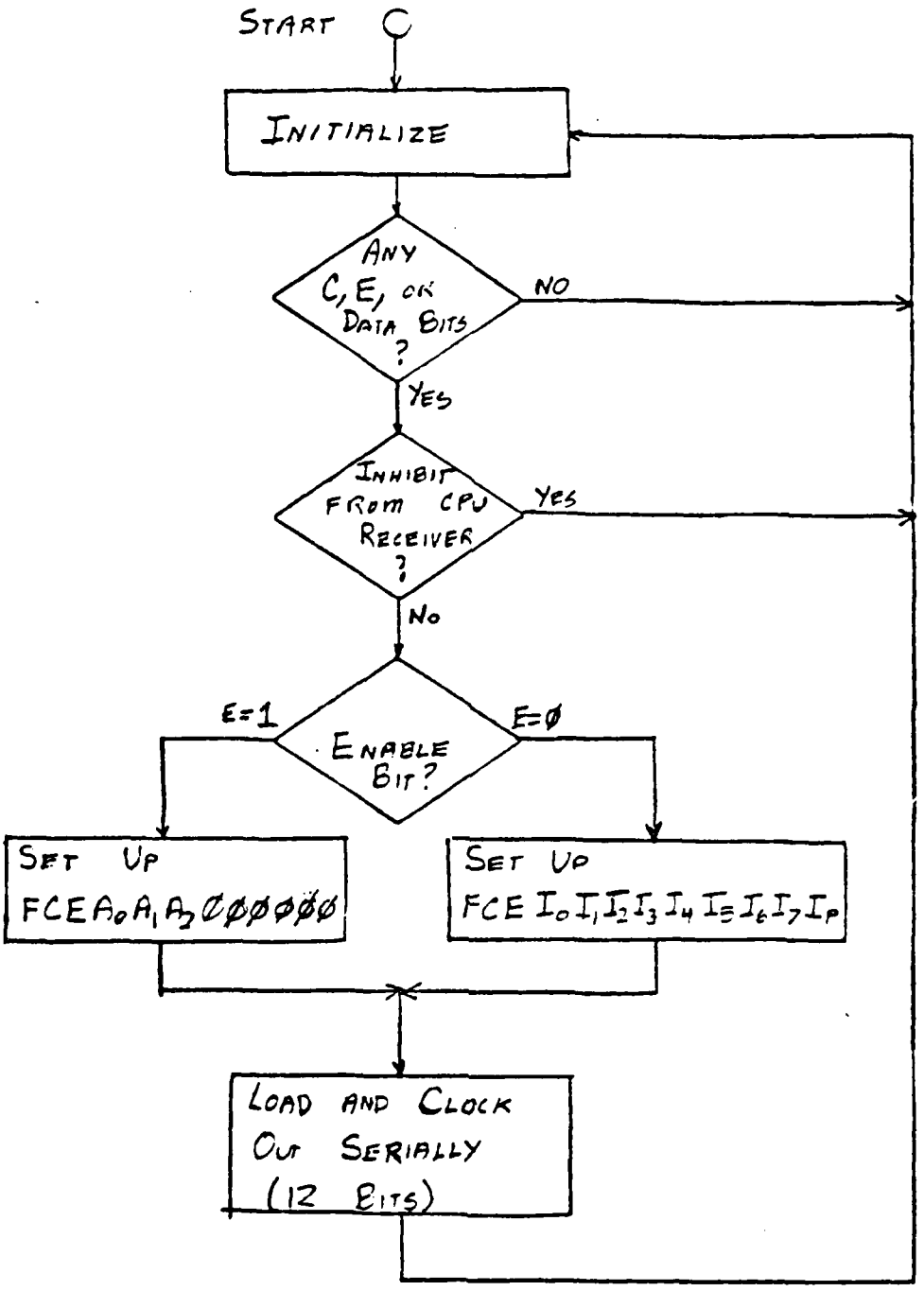


Figure 3-3 CPU Transmitter Logic Flow

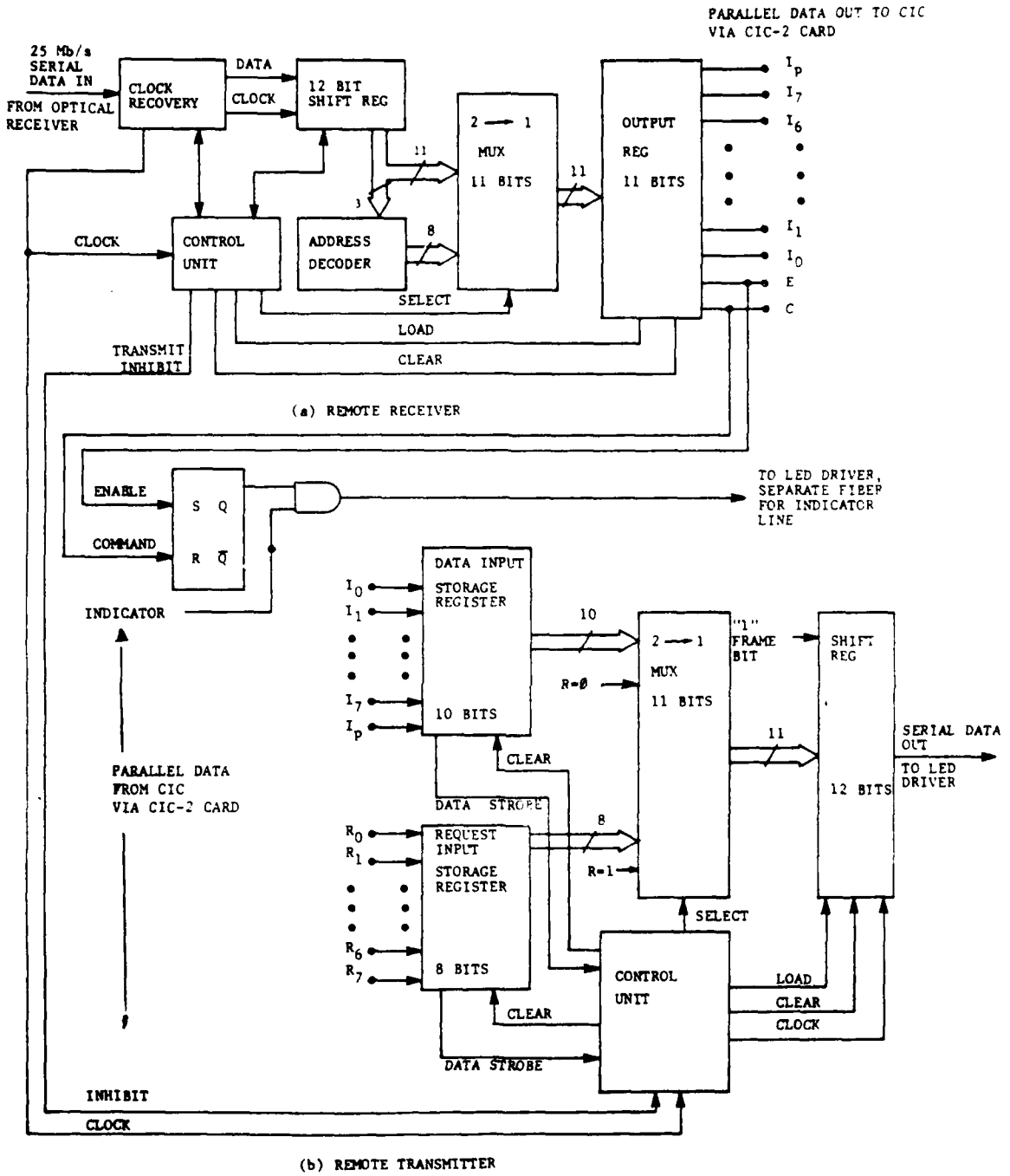


Figure 3-4. Remote Transmitter/Receiver

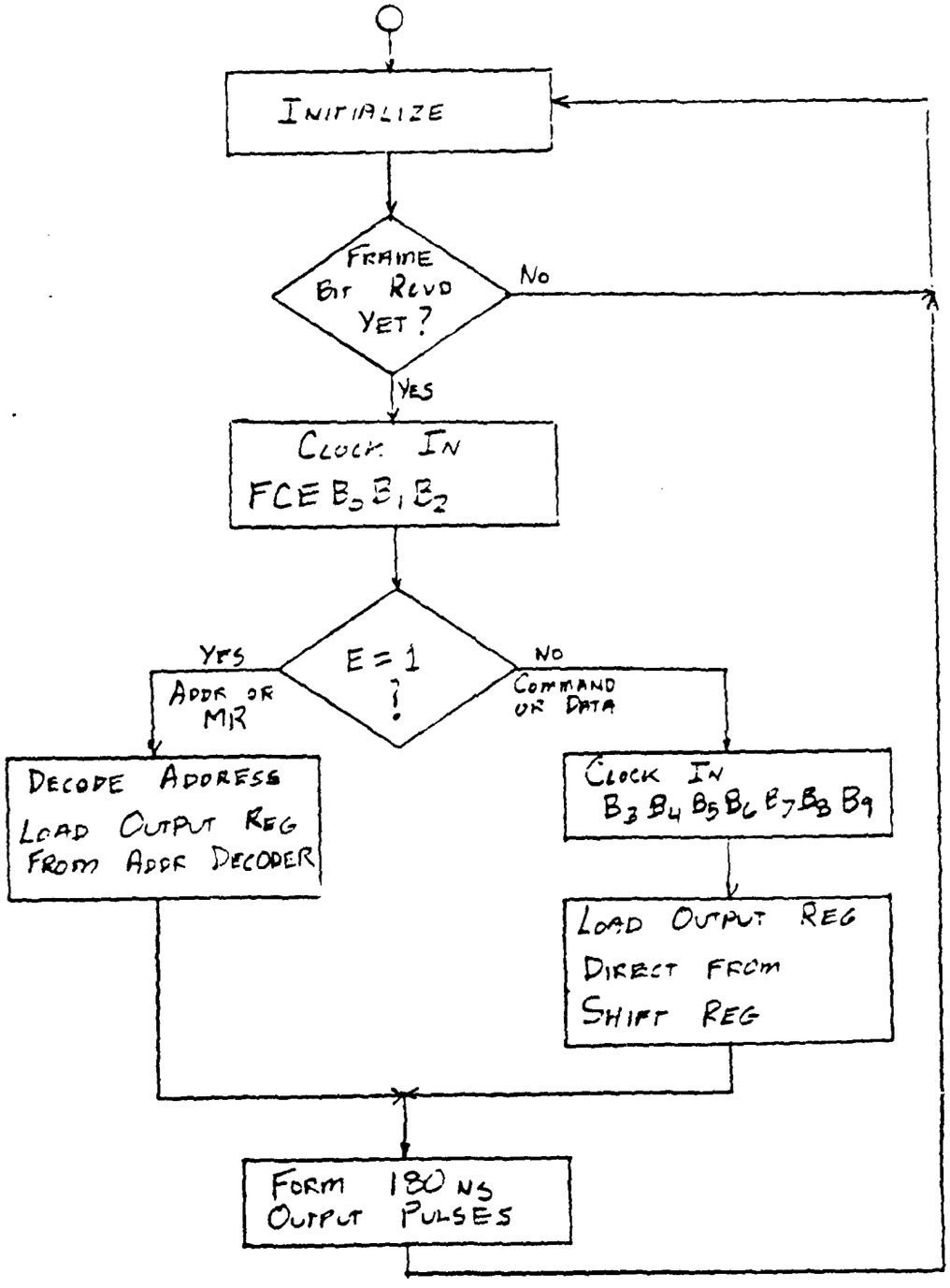


Figure 3-5 Remote Receiver Logic Flow

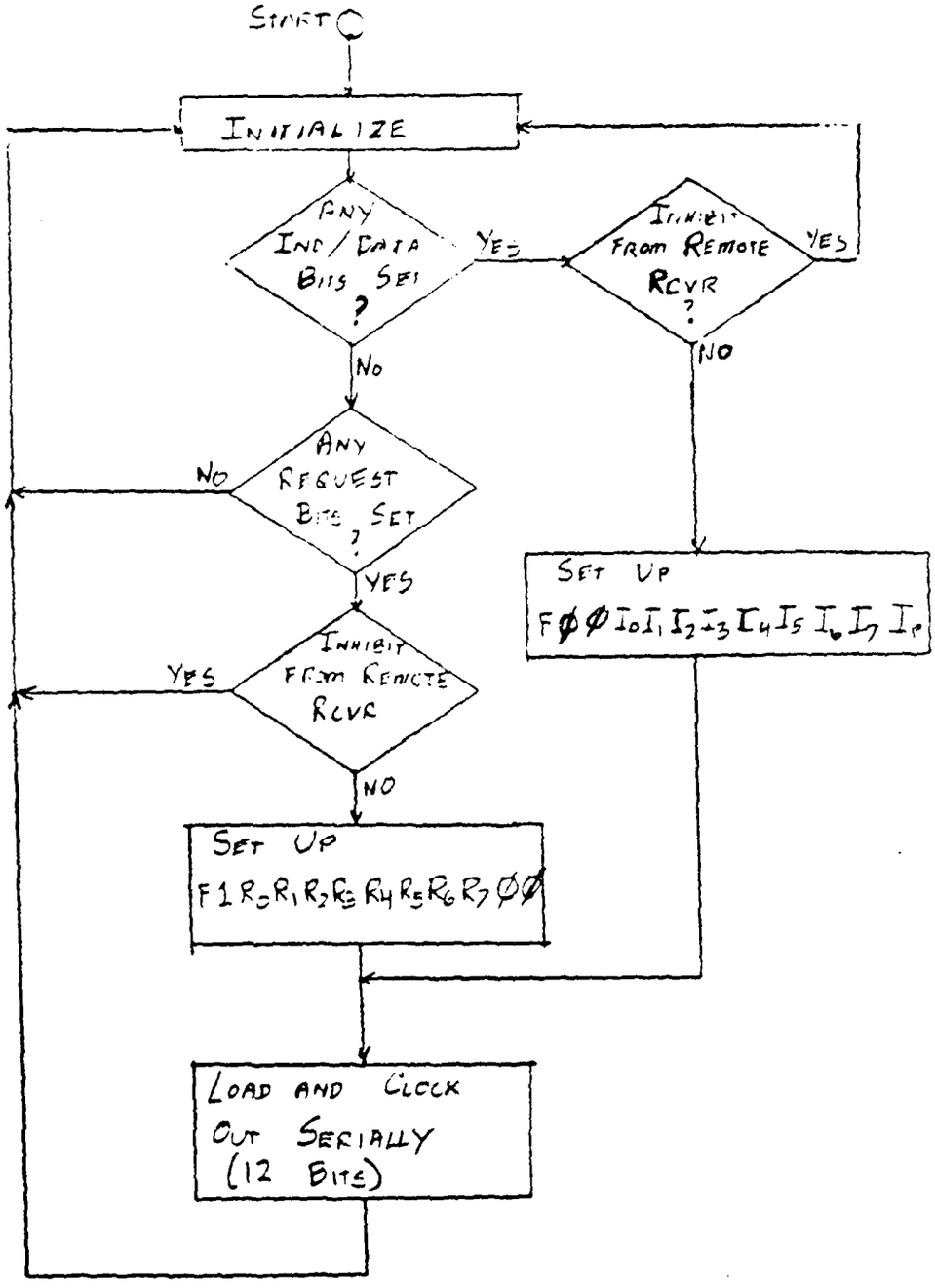


Figure 3-6 Remote Transmitter Logic Flow

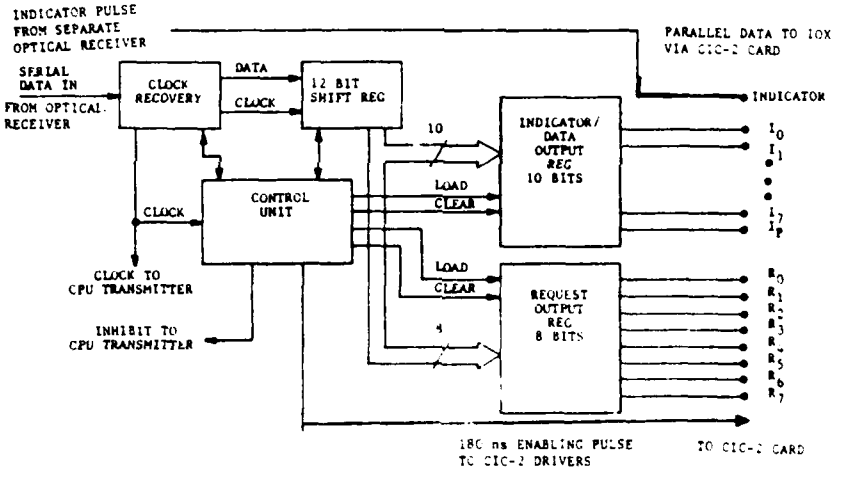


Figure 3-7. CPU Receiver

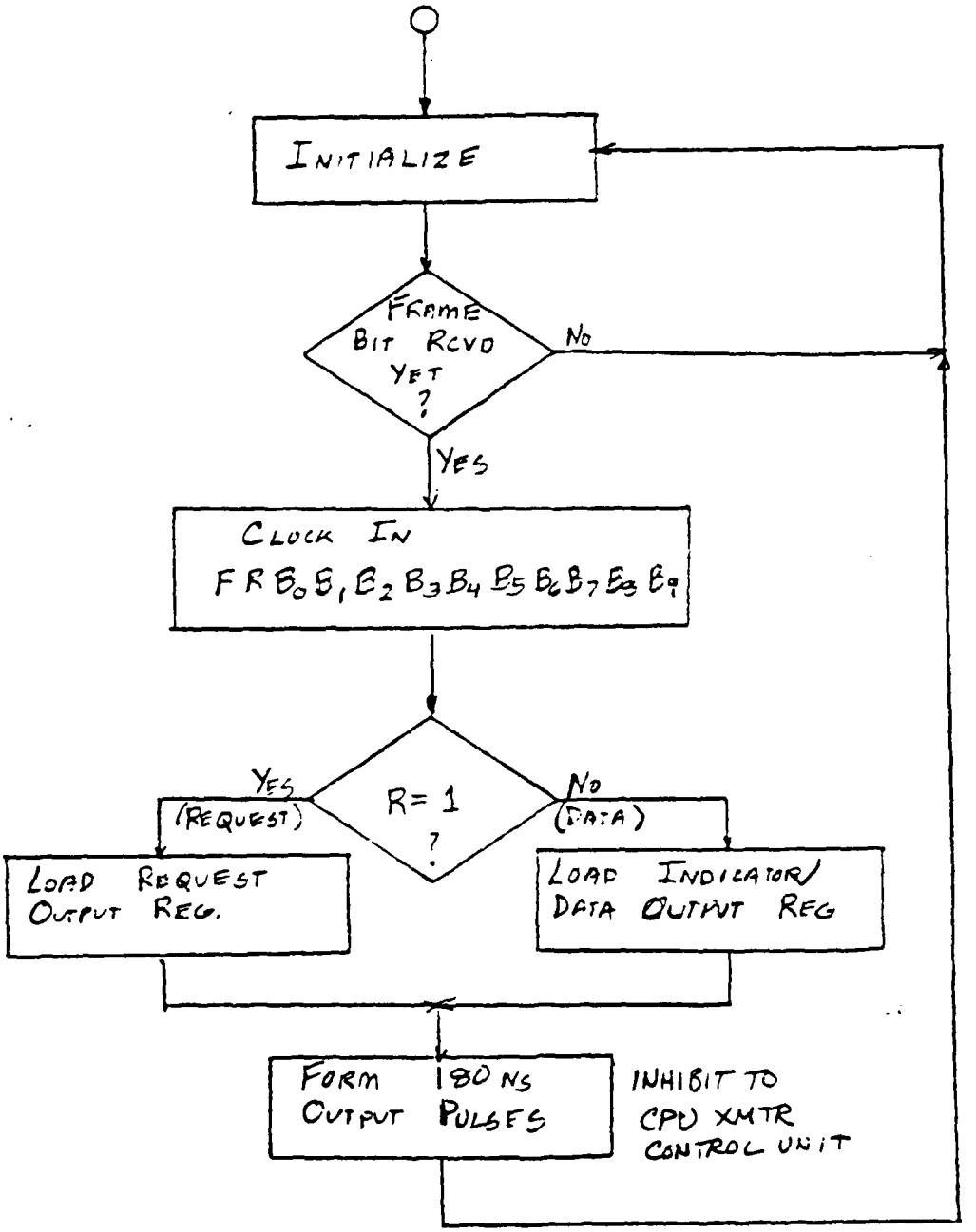


Figure 3-8 CPU Receiver Logic Flow

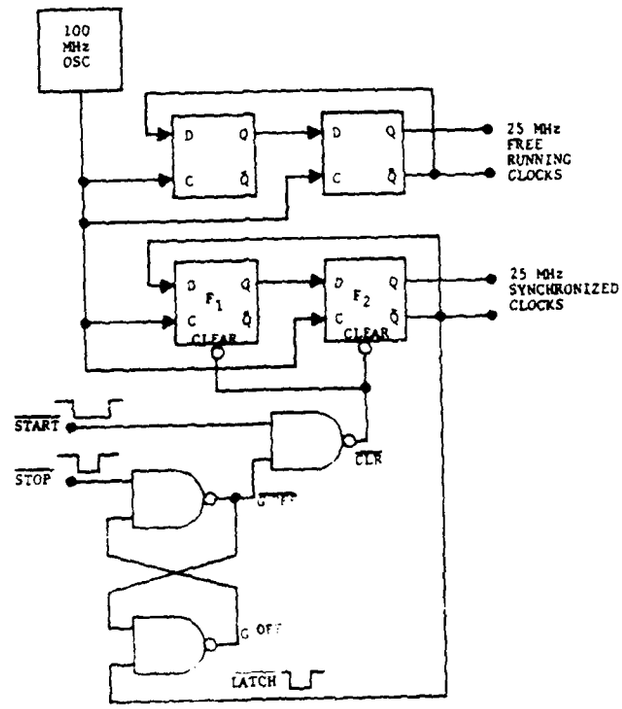


Figure 3-9. Clock Recovery Logic

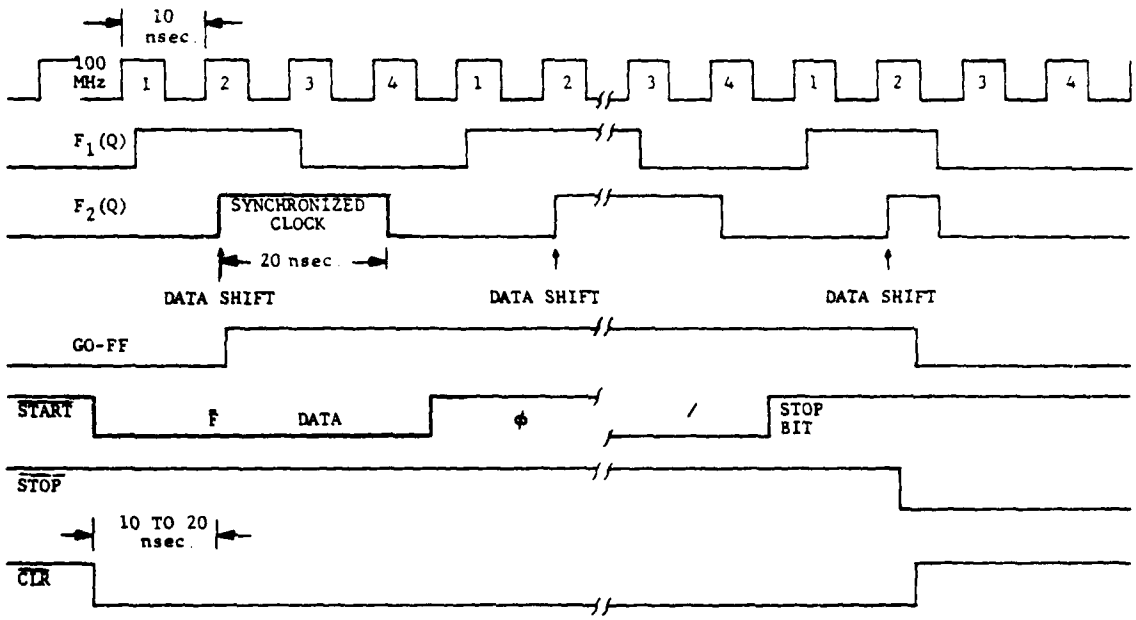


Figure 3-10. Clock Recovery Timing

flow specified by the control flow diagram. The framing bit is forced into the first-out position and the stop bit is formed by the return-to-zero caused by the emptying out of the last data bit in the shift register. The data strobe is formed by the logical OR of C, E, and I_n lines, which have a timing dispersion such that the data strobe can be as short as 150 nanoseconds or as wide as 290 nsec out of a 550 nsec period.

The Control Unit receives a logic level from the CPU Receiver control which is used as an "ignore-data" signal during the time that the CPU Receiver is delivering data towards the processor.

3.1.1.1.2 Remote Receiver (CIS Nest)

The data bit stream from the receiver on the Optical Modem card (MPS to CIS fiber) is applied to the input to a 12-bit serial shift register. Clock is recovered from the data stream by the technique described in Section 3.1.1.1.5. The resultant clock pulse, synchronized and properly time-phased with the data bit stream, is used to gate the bits into the first stage of the shift register as well as provide shift pulses until all the data is shifted in. If 25 megabits/sec is used, all pulses are in the shift register within 520 nsec (one processor clock period) in a 12-bit transmission. According to the control flow, a ONE-state E-bit (second bit received) specifies an Address or Master Reset, and transmission is complete within a 6-bit transmission. For a ONE state E-bit, the three address bits are decoded and loaded into the parallel Output Register. For a ZERO-state E-bit, the 12-bit transmission is received and loaded without modification and is ready to be gated onto the IOX lines toward the device. The CIC-2 card forms the 180 ns pulses from the logic signals supplied by the receiver card.

If E-bit was received as a ONE, a transmission gate is enabled to pass the device INDICATOR bit back to the processor via the INDICATOR fiber path. This path will be used for the transmission of INDICATOR signals except for the ALARM mode operation described below.

3.1.1.1.2.1 Alarm Mode Operation

The Alarm Mode operation is used by the MPS processor to count events that are represented by a device request. The processor acknowledges the device requests with an address selection phase employing the ENABLE line. There is no data transferred in this mode. The block length register in the keyword associated with the device is decremented each time a request is received. A peripheral device that uses this mode may generate an interrupt sequence if the INDICATOR signal is returned less than 700 ns after the enable signal is received.

The TYC-39 Message Switch software uses the Alarm mode for the following:

a. CAP/VDU Logic in the MP Shelter
b. Non-active Devices
c. CICM Channel 2 in CI Shelter.

The only condition above that is affected by the LDFOCCS system is (c), since the CICM is located in the CI shelter and since CICM CHannel 2 generates interrupts while in the Alarm mode. The LDFOCCS hardware results in a delay in the communication path between the MP and CI shelter in excess of 700 ns. Therefore, the interrupt generated by CICM Channel 2 would be missed by the processor if the normal INDICATOR channel were taken. The LDFOCCS IOX-T hardware, therefore, automatically simulates an INDICATOR signal to the processor whenever it detects an address selection phase employing the ENABLE line from the processor to CICM Channel 2. This does not affect the use of the normal INDICATOR channel for the other functions, i.e., DEV. OFR, and ITR commands.

The automatic simulation of the INDICATOR signal presents the possibility of the following situation. If the INDICATOR line in the CICM fails right after a request from Channel 2 was initiated, then the LDFOCCS hardware would return the INDICATOR even though it did not receive it from the CICM. This will not mask a failure, however, since the normal INDICATOR channel is used for all of the other I/O functions in the CICM, and this failure would be detected the next time there was any communication with the CICM. The fact

that the INDICATOR was sent instead of being missed because of the hardware failure does not pose any problems. It actually ensures that the interrupt status byte that is sent with the INDICATOR is received by the computer, whereas it would have been lost if the INDICATOR had not been sent.

3.1.1.1.3 Remote Transmitter (CIS Nest)

As in the CPU transmitter, input data storage registers are required to hold the parallel information transmitted from the CI shelter end of the IOX Link. Within the specified "skewing" window Information lines are logically ORed to form a data strobe. The same applies to any one of the eight Request lines entering their Request Input Storage Register. The Control Unit observing the content of both registers upon the first non-zero occurrence will take action on the Data Input Storage Register as first priority. As long as there has been no inhibit level from the Remote Receiver (Information moving in opposite direction), the Control Unit will transfer the Data Input Storage Register through And-Or-Select gates into the Shift Register with the R-bit position forced to a ZERO state and the F-bit position forced to a ONE state to conform to the format shown in Figure 3-1. Once the LOAD is accomplished, Serial Data Out shifting is accomplished at the local 25-megabit rate (free running clock in Figure 3-9 starting with the F framing bit and ending with the last bit leaving the register). As in the CPU transmitter, the end of transmission from the transmit point of view is the last return to ZERO.

If the Request Input Storage Register had been the first non-ZERO register from the point of control initialization, the Control Unit would have instead transferred its contents via And-Or-Select gate (2/1 MUX) into the Shift Register, while forcing the F and R bit positions to ONES and shifting out a character in the format indicated in Figure 3-1. In this case, the trailing ZEROs are inserted in the last two bit positions of the Shift Register.

3.1.1.1.4 CPU Receiver (MPS Nest)

The serial bit stream from the receiver on the Optical Modem card (CI to MP shelter) is applied to the input to a 12-bit serial Shift Register. Clock is generated locally, started and phased by the F-bit as described in Section 3.1.1.1.5, and used to shift in the data. Once the F-bit has reached the end of the register (register full), the Control Unit transfers the data in parallel to either the Indicator/Data Output Register (10 bits) or the Request Output Register (8 bits), depending upon the state of the R-bit while still in the Shift Register. In the Output Register, the parallel information is available to be gated onto the IOX lines toward the processor via the CIC-2 card. The Control Unit provides a timed enabling pulse for this function.

3.1.1.1.5 Clock Recovery Logic

Figure 3-9 shows the method for producing a series of clock pulses which will be properly phased with an incoming serial bit stream. The starting and phasing process takes place within one-data-bit time and will always position the leading edge of the clock pulse (initially) between the 25 and 50 percent points of the data bit period. A crystal oscillator free-runs at four times the data bit frequency. A four-state counter is constructed of two D flip-flops, the second FF of which provides the synchronized clock pulse. The CLEAR inputs of the FFs are initially holding the counter OFF.

When the F-bit is received (START'), the CLR' gate goes HIGH releasing the counter to start counting. After the second oscillator pulse, the GO-FF is SET, thereby holding the CLR' gate OFF for the remainder of the bit stream regardless of the state of START'. The clock is inhibited by receiving the STOP' pulse, which is generated by sending the F-bit in its final resting position in the Shift Register.

Refer to Figure 3-10 for a timing diagram of this circuit. Note that the GO-FF has only 10 nanoseconds to be reset to stop the clock at the proper time. Delays in this logic area must be carefully considered.

3.1.2 Optical Modems

The optical modems accept T^2L digital data and deliver T^2L digital data over a range of 1.152 to 30 Mbps with a BER $\leq$ 5×10^{-11} and a path length of 38.1 meters. Since the optical fiber's attenuation ($\leq$ 10 dB/Km) and dispersion (typically 1.6×10^{-9} s/km) are small at this length, the power losses are largely a function of the connectors used. Based upon the specified connector loss ($\leq$ 1.8 DB/connector), the total connector loss if $\leq$ 7.2 dB, it was shown that an LED source should provide sufficient power for a PIN diode receiver.

Schottky T^2L logic circuitry was used to meet the power-speed requirements. A common receiver and a common transmitter circuit design is used to accommodate all of the signals. The optical modem card was designed to accommodate three receivers and three transmitters with a single card-edge connector, which will provide both electrical and optical connections from the card to the nest/cable/wiring. The optical modem, as shown in Figure 3-11, provides for three IOX communications on three fibers and C/S communications on two fibers and a spare transmitter on one card connected to a spare receiver on the other card. Thus each modem is alike and one is used per shelter. (Note: a second, identical card is provided in each shelter for standby or off-line use.)

3.1.2.1 Optical Transmitter

The optical transmitter schematic is shown in Figure 3-12. This consists of a Schottky T^2L driver (54S37), which drives a Laser Diode Labs Burrus type LED (SCS-511) to a peak forward current of 60 mA. A speed up capacitor is used to reduce delay and optical rise time. Since the 54S37 actually contains four drivers per package, the full modem cards complement plus a spare is provided by the one package, saving valuable card real estate.

A logical ONE at the driver's input causes the LED to conduct in the forward direction; the driver is non-inverting in the sense that an electrical logical "ONE" input ($V_{IN} \geq 2V$) causes an optical "ONE" output as characterized by a rise in LED optical output.

The peak steady-state forward current for the LED is given by:

$$I_F = \frac{V_{CC} - V_{SAT} - V_D}{R_1}$$

where V_{CC} = 5V, V_{SAT} = 54S37 logical ZERO output voltage $\leq$ (0.25V), and V_D is the LED forward voltage drop ($V_D \approx 1.9V$ @ I_F = 60 mA). The value of R_1 for I_F = 60mA is 47 ohms

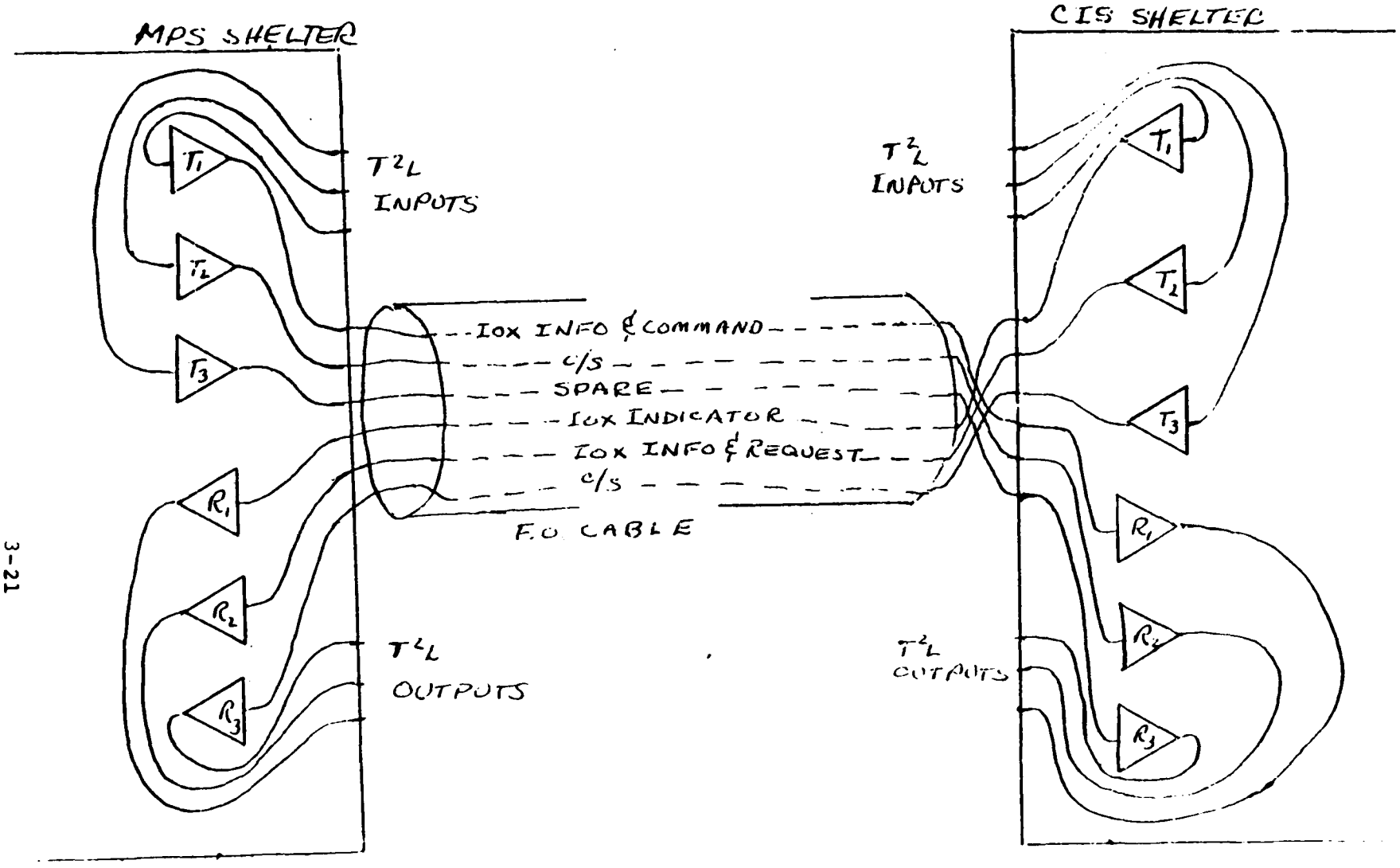


Figure 3.-11 Optical Modem

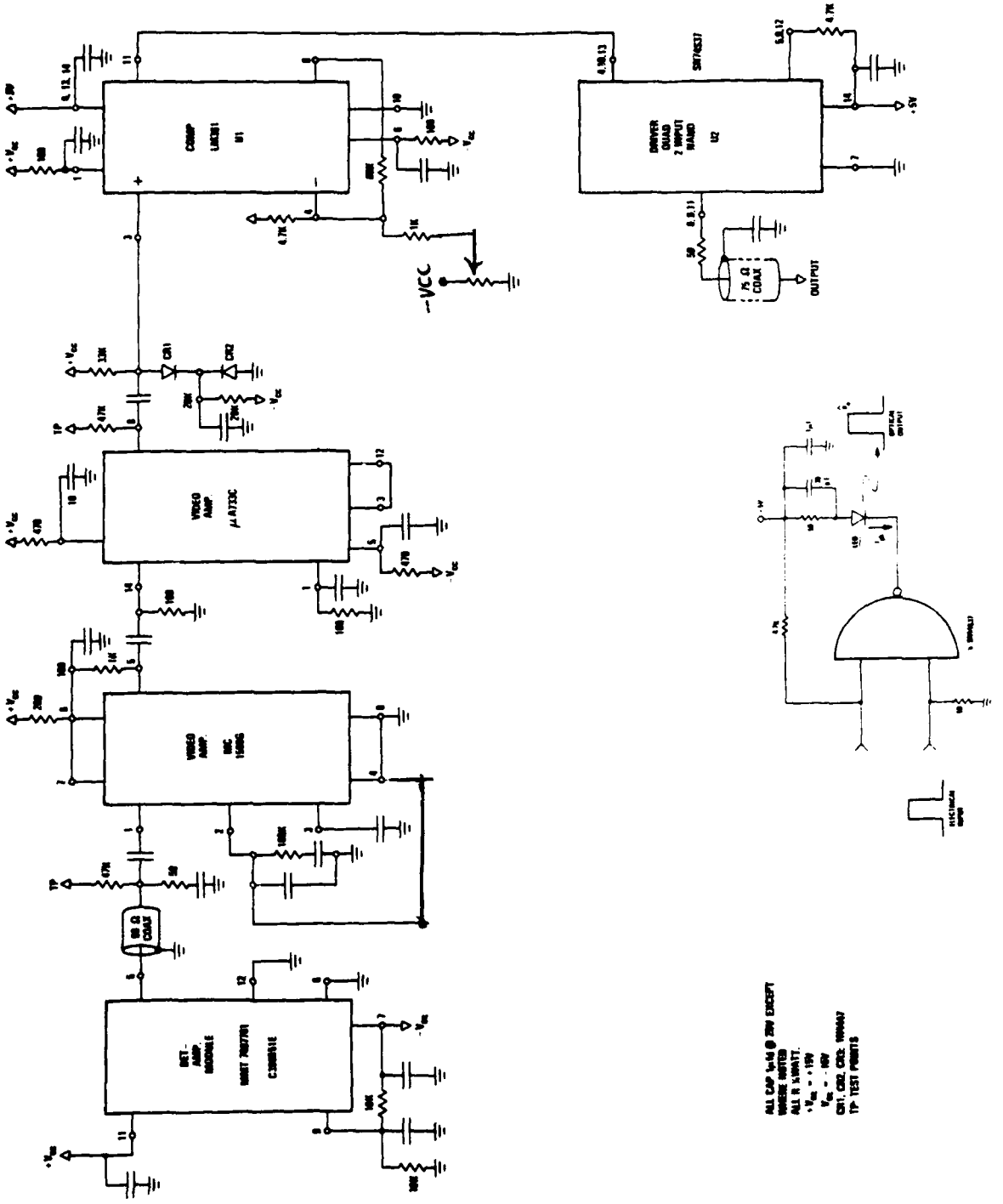


Figure 3-12. Optical Transmitter/Receiver Schematic Diagram

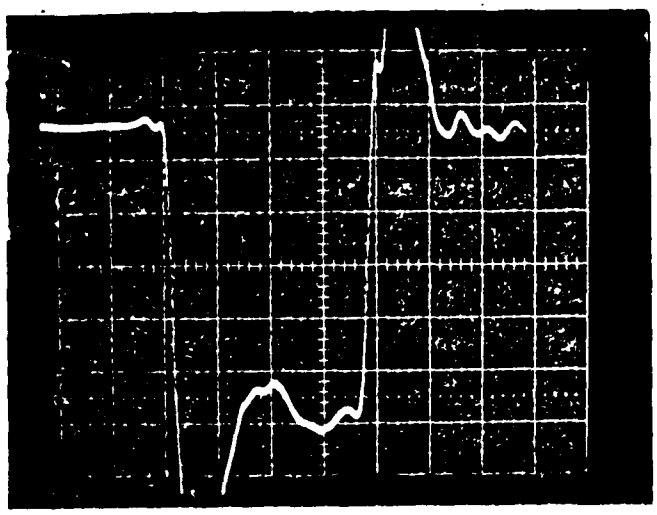
The value of the peaking capacitor is chosen so that the time constant (R_1C_1) is approximately one-half the LED uncompensated rise time. For an uncompensated rise time of 15 nsec the value of C is 160 pf. LED current rise and fall times are shown in Figure 3-13.

The driver input is terminated in 75 ohms to match the characteristic impedance of the 75-ohm coaxial transmission line.

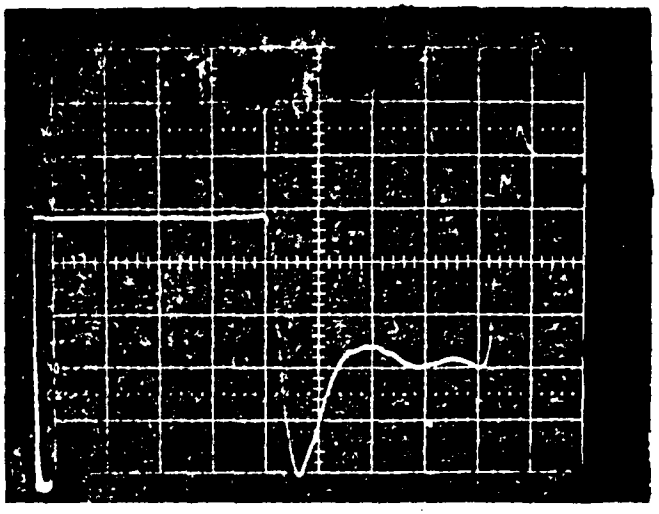
3.1.2.2 Receiver Design

A single receiver design is used for both C&S and IOX signals. The receiver accepts digital optical signals at bit rates between 1 and 30 Mbps and converts them to T^2L logic. The receiver's output will be non-inverting so that complete "transparency" exists between the transmitter input and the receiver output (i.e., a "ONE" or a "ZERO" transmitter input causes a "ONE" or a "ZERO" receiver output).

The receiver diagram is shown in Figure 3-12. The optical input to the PIN detector causes an output voltage at the Detector/Amplifier module. This signal is amplified by the two video amplifiers and applied to Input A of the comparator. When the signal voltage exceeds the dc threshold level at input B, a logic ONE appears at the output, and when the signal level at A is less than the threshold level at B a logical ZERO is produced.

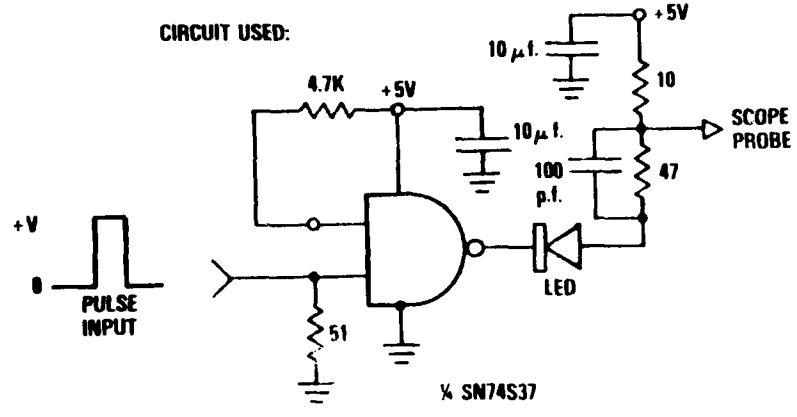


(a)



(b)

$t_r = t_f \simeq 5$ nsec



(a) 0.1 V/cm
10 nsec/cm

(b) 0.2 V/cm
10 nsec/cm

Figure 3-13. LED Rise, Fall Times

Since the receiver is designed for both the C&S and the IOX links, it handles a variety of signals. The extremes of these signals are summarized in Table 3-2.

TABLE 3-2. RECEIVER OPTICAL INPUT SIGNALS

C&S Link: (RZ),PRR = 1.152 Mbps, P.W. = 217 nsec.
IOX Link: (NRZ), Bursts of 40 nsec pulses in 550 nsec period.
IOX Link: Max. P.R.R. = 25 Mbps, P.W. = 40 nsec
IOX Link: Min. P.R.R. = 1.92 Mbps, P.W. = 40 nsec
IOX Link: Min. P.R.R. = 1.92 Mbps, P.W. = 480 nsec
Min. Peak Power Required for BER of 5×10^{-11}:
(Typical) $P_{IN} \geq 0.4$ μW
(Worst-Case) ≥ 0.8 μW

Since the worst-case available power at the detector is approximately 1.8 μW (See 3.1.2.3), there is sufficient power available at the detector's input.

The peak output voltage of the detector/amplifier module (V_{01}) is the product of responsivity and input power. For $P_{IN} = 1.8 \times 10^{-6}$W, $V_{01} = 5.8 \times 10^{-3}$V. The output impedance is $\leq$50 ohms.

The voltage gain (VG1) of the MC-1590G video amplifier is directly proportional to the load resistance (R_L), while the bandwidth is an inverse function of R_L. Using a value of R_L = 100 ohms, the voltage gain is 20 dB (10) and a 3-dB bandwidth is is approximately 70 MHz. The input impedance for the MC1590G consists of a shunt resistance, which varies from 4K to 1.43K between 10 MHz and 70 MHz, and a shunt capacitance, which varies from 14 pf at 10 MHz to 7.7 pf at 70 MHz.

Since the output impedance of the detector/amplifier module is less than 50 ohms, the MC1590G does not load down the detector/amplifier, and the output voltage of the MC1590G is 45×10^{-3}V (peak) into a load much larger than R_L (i.e., open circuit). The output of the MC1590G is fed into the μA733 video amplifier operating with gain 2 conditions (i.e., VG = 50). Since the input impedance of the 733 is a parallel combination of 30K resistance and 2 pf capacitance, its loading effect upon the MC1590G (R_o = 100 ohms) is insignificant. The output voltage of the 733 operating with a voltage gain of 50X is approximately 2.25V into a load greater than 20 ohms. Since this is less than the limit of the linear output voltage swing (4V typical), pulse fidelity is preserved (the 733 3-dB bandwidth is 90 MHz), and a very fast rise and fall time pulse with large overdrive is presented to the input of the comparator. The pulse's dc level is clamped to zero, using a zero-level clamp at the comparator's input.

The comparator (LM161D) is capable of less than 5-nsec rise and fall times with very little delay variation, and has a T^2L Schottky output. The input impedance of the comparator is high ($R_{IN} \leq 20K$) compared to the 733 output impedance ($R_o \leq 20$ ohms), so that no significant loading of the 733 output occurs. The signal is applied to input A and a dc voltage equal to one-half the peak signal amplitude (+1.12V) is applied to input B. It is felt that the very fast rise and fall times of the pulses at input A and the relatively low noise voltages on the signal as well as the threshold level at input B will reduce temporal jitter, so that no strobe pulse will be required, and the 161D strobe inputs may be grounded.

Hysteresis (positive feedback) is used in the comparator circuitry to guard against noise-induced false threshold crossings. The hysteresis also tends to reduce turn-on and turn-off times, so that the operating point spends very little time in

the active region, thus reducing any tendency toward self-oscillation. The hysteresis voltage (difference between upper and lower triggering levels) is equal to the ratio of the input resistance to the sum of the feedback and input resistances and is adjusted via a potentiometer.

3.1.2.3. Link Power Budget (Worst-Case)

The link power budget is the accounting of the optical power as it moves from the source (LED) to the receiver (PIN detector).

The power available from LED is the optical output power from the LED fly-lead into the first of the four optical couplers. From measurements made on the Laser Diode Labs light-emitting diodes, it appears that approximately 50×10^{-6} W (best-case) is available at room temperature and the forward bias current, I_F = 100 mA. For worst case, it is assumed that 45×10^{-6} W output is available at 25°C. If one assumes a 10 percent reduction for operation at 52°C and a 40 percent reduction for operation at a reduced forward bias current (I_F = 60 mA) to ensure adequate lifetime and allow for the use of the Schottky T^2L 53S37 driver, the maximum available power from the LED fly lead is 24×10^{-6} W. Assuming a 2-dB coupler loss when coupling fibers with the same characteristics, the total coupler loss is 8 dB (four couplers). The fiber loss is assumed to be 0.3 dB (i.e., 0.03 km of 10 dB/km fiber), and a 3-dB margin is allowed. These losses and the power available at the detector are tabulated:

Power Available:	$P_{LED} = 24 \times 10^{-6}$ W (I_F = 60 mA, T_A = 52°C)
Normal Coupling Loss:	8 dB (4 couplers at 2 dB each)
Fiber Loss:	0.3 dB (0.03 km at 10 dB/km)
Margin:	3 dB
Total	11.3 dB
Power Available at Detector:	1.8×10^{-6} W

3.1.2.4 Card Partitioning and Design

There are several driving forces that influence the partitioning of optical transmitter and receiver circuits on cards:

a. Total number of fibers utilized
b. Number of fibers in each direction
c. Redundancy requirements
d. Number of circuits that will fit on a card
e. Ease of interfacing fibers to cards
f. Fault isolating capabilities employed.

The minimum number of fibers required is three for IOX Link A, three for IOX Link B, and two for C&S link, the total indicating the use of two 6-fiber standard cables. To produce redundancy consistent with the present wire cables, IOX fibers are located in two cables. With the remaining fibers available optical system redundancy was provided by adding a steering toggle (on edge of RCHYB PCB) which will allow selection of a XMTR/RCVR pair at each end of the link. The toggle is used to steer the single INPUT and OUTPUT serial bit streams between the DGM card and the two different XMTR/RCVR pairs.

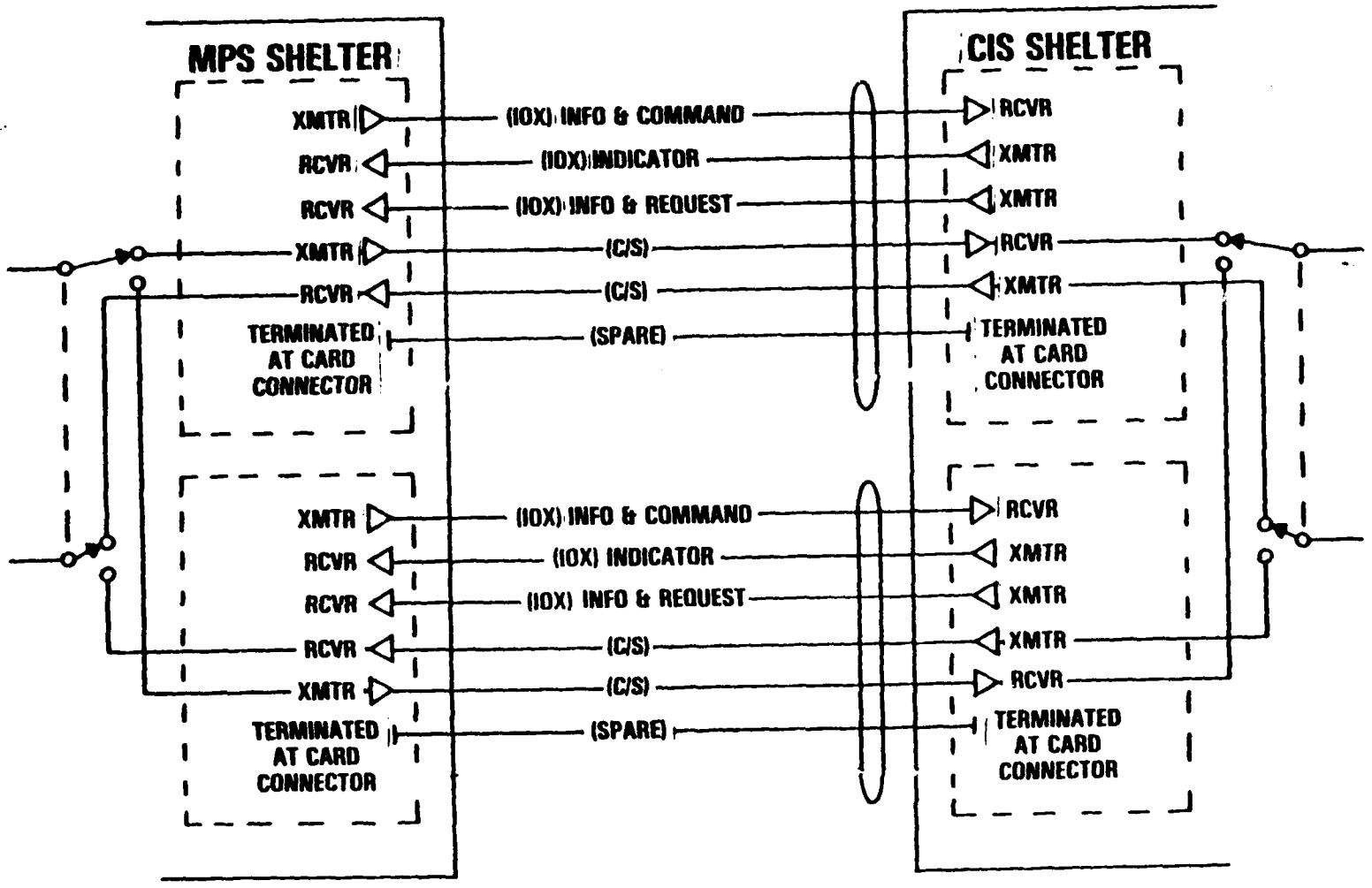


Figure 3-14 Optic Modem Partitioning

3.2 Communication and Status Link Electrical Design

3.2.1 Multiplexer Subsystem

The interface between MP and CI shelters contains 23 various types of signals including intercom, TA-341 and DSVT telephone sets, teletype, ALARM, SELECT, and STATUS levels. All signals are converted, if necessary, into digital form at the bit rate of the highest rate requirement of the group, and then multiplexed, framed, and modulated prior to presentation to the optical fiber system. The reverse process is applied at the receiving end to restore signals to their original form, such that the individual signals have traveled through a transparent path from one shelter to the other. The design is the use of the DSVT bit rate of 32 kb/s as the standard channel rate, and use the nearest modular number of channels presently available in the Nine-Channel Mux/Demux (NCMD) card. Allowing for spare channels and a framing channel, the number 36 was chosen. This will arrive at a multiplexed bit stream of 1.152 mb/s.

3.2.1.1 Subsystem Description

Table 3-3 depicts all major hardware elements used in the C&S link. These elements are interconnected as shown in Figure 3-15 Standard TTC-39 cards have been chosen wherever possible in the implementation of this link. DGM, TGM, and NCMD cards form the basic subsystem. Following the functions from parallel to serial. the successive cards bring all signal lines up to 32 kb/s for presentation to the NCMD card inputs. Intercom hybrid circuits provide the conversion from a two-wire bidirectional audio path to four-wire transmit and receive pairs on the RCHYB cards. The TA-341 telephone set is already in this form. Both TA-341 with its signalling and supervision tones, and the two intercom four-wire outputs are brought to CVSD cards where audio/slope delta conversion is performed in both directions. The group of Select,

TABLE 3-3. CARD LIST

Design Type	Name	MPS Qty	CIS Qty	Comments
Standard	Diphase Loop Modem A (DLM A)	1	1	
Standard	Continuously Variable Slope Delta Modulator/ Demodulator (CVSD)	2	2	
Standard	Nine-Channel Multiplexer/ Demultiplexer (NCMD)	3	3	
Standard	Group Buffer (GRPBF)	1	1	
Standard	Group Framing (GRPFR)	1	1	
Standard	Group Output Control (GRPOT)	1	1	
Standard	Diphase Group Modem (DGM)	1	1	Output circuitry removed and jumpering to card edge connector for direct TTL interface with Optical Modem card.
Standard	Local Timing Generator (LTG)	1	1	
Standard Topology	Line Driver/ Receiver (LNDR)	1	1	Standard TTC-39 circuits on new layout PCB to cover circuit quantity requirements.
New	Resistor/Clock/ Hybrid (RCHYB)	2	2	Has resistor terminations, clock oscillator for LTG, and Intercom Hybrid/Direction Control
New	IOX-Xmtr	2	2	Used at either end by PCB straps or rear-wiring differences.
New	IOX-Rcvr	2	2	Used at either end by PCB straps or rear-wiring differences.
Standard	CIC-2	2	4	
New	Optical Modem	2	2	

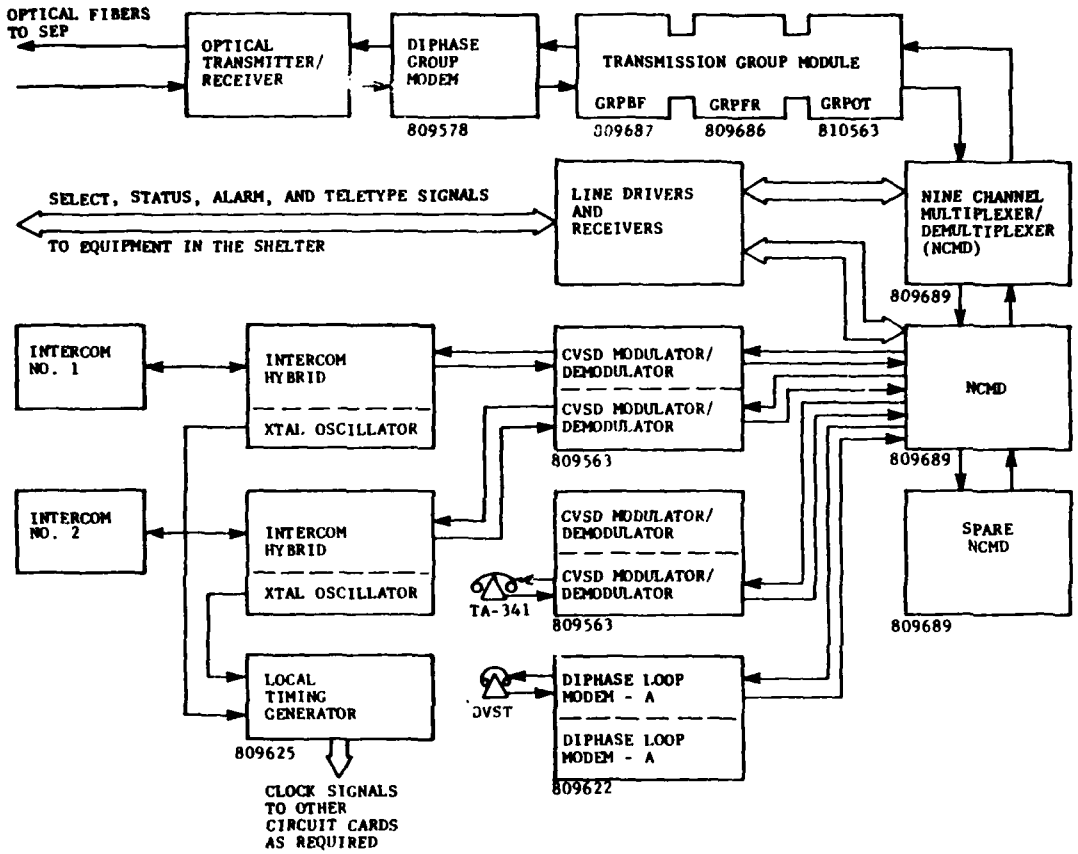


Figure 3-15. Block Diagram of Communications/Status Link

Status, Alarm, and Teletype signals are brought through a set of line drivers and receivers utilizing standard TTC-39 circuits on a new card type. This collection of signals is comprised of mainly DC levels and a 200b/s TTY four-wire circuit. The DSVT telephone set is brought through a DLM-A card, which performs the diphase/baseband conversion on a four-wire basis, and brings signals to levels compatible with NCMD interface. All signals now having been made compatible with the NCMD, the resulting 32 kb/s channels are multiplexed into a single 1.152 mb/s bit stream and applied to the Transmission Group Module. This three-card group is basically responsible for generating the initial framing of channels, testing for frame sync, generating of framing request when sync is lost, and maintaining a clock drift FIFO of the serial bit stream. The output of the TGM group connects to the Diphase Group Modem card (DGM), which performs the baseband/diphase conversion as well as clock insertion/extraction. This card is stripped of its normal long-line driving and receiving circuits, and is connected instead at a TTL compatible level point to the Optic Transmitter/Receiver card. A Local Timing Generator (LTG) card performs a frequency-divider-type operation from clocks located on the RCHYB card and provides synchronized timing to all the cards in the group described above, with the exception of LNDR and RCHYB cards. Each card function is described in more detail in the subsequent sections with emphasis on the new card design types.

3.2.1.2 Card Descriptions

3.2.1.2.1 Diphase Loop Modem - A (DLM-A)

The Diphase Loop Modem consists of a Modulator and a Demodulator as shown in Figure 3-16.

Loop Modem Modulator - accepts baseband data at 32 kb/s (or 16 kb/s) and converts the baseband data to conditioned diphase data.

Data Modulator - The baseband data in from the NCMD demultiplexer is sampled by a standard clock. The data is conditioned so that there is a transition whenever the data is a logic ONE at the sample time. The conditioned data is module-two added with the 32 kHz square-wave clock in an exclusive-OR gate. The resulting output is a conditioned diphase signal that changes phase whenever a logic ONE is transmitted. Output sliver spikes due to squarewave/conditioned data differential delays are eliminated by reclocking the diphase signal with a 64 kHz squarewave. The reclocking flip-flop is inhibited whenever there is a lack of baseband data activity and diphase carrier, thus inhibiting the DLM-A diphase data output.

Line Driver and Transformer - The Line Driver accepts diphase data from the Data Modulator and transmits it down the field wire. An open collector gate provides a stable squarewave which is then AC coupled into a current driver with unity voltage gain. A transformer is used to couple the 2.0 volts peak-to-peak diphase signal to the field wire. The output impedance is 125 ohms.

Data Activity Detector - The detector consists of a retriggerable one-shot. Baseband activity results in transitions which constantly retrigger the one shot for each input ZERO and result in a logic ONE at the one-shot output. No baseband activity results in loss of data transitions causing the one shot to change state after the timeout period established by the external RC network. The timeout period is 1 to $\pm$0.5 msec.

Loop Modem Demodulator - The DLM-A accepts conditioned diphase data and converts to baseband data.

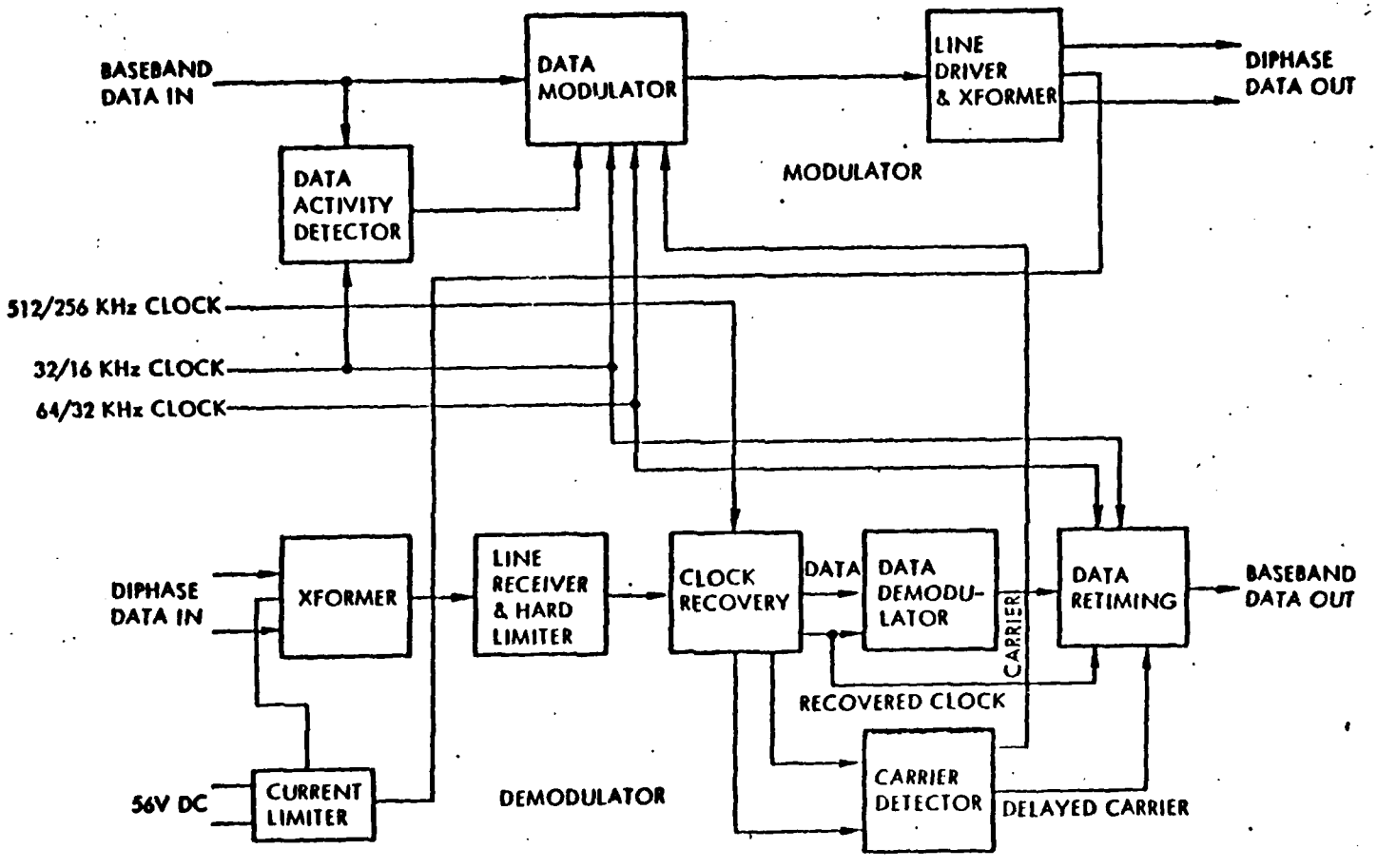


Figure 3-16 Diphase Loop Modem-A Block Diagram

Line Receiver and Hard Limiter - The diphase signal on the field wire is applied to a transformer coupler into an op-amp which incorporates a one-pole filter for noise suppression. The filter output is then applied to a digital comparator (hard limiter) which requires a low level differential input in order to switch states. The input impedance of the demodulation is the field wire characteristic impedance (WF-16).

Clock Recovery Circuit - The clock recovery circuit contains a shift register which produces delayed data signals. Two delayed data signals are exclusive-ORed to produce a signal with a frequency component at twice the data rate. This signal is coupled to a phase-locked loop that produces a stable recovered clock.

Data Demodulator - The data and a clock signal are exclusive-ORed together to obtain conditioned baseband data. The data is deconditioned by exclusive-ORing the outputs of a two-bit shift register.

Data Retiming Circuit - The incoming data phase is a function of field wire length and can be at any phase with respect to the local clock. In order to avoid sampling received data on a transition edge, a clock phase selection circuit is implemented. The diphase data is sampled by the proper clock phase. Baseband data is clocked out of the DLM-A on the rise transition of the local clock. The output data is enabled by the Carrier Detector output. When no carrier is present, the DLM-A outputs a constant logic ONE.

Carrier Detector - The Carrier Detector determines whether or not a carrier is present on the input diphase line. The "carrier" output, which occurs 5 to 60 msec after an input carrier is received, allows a diphase output signal to be transmitted. The "delayed carrier" output, which is delayed 180 $\pm$ 50 msec from the "carrier" output, activates the data retiming circuit to select the proper phase of the local clock and enables the baseband data output. Within one second after the diphase input ceases, the "carrier" and "delayed carrier" signals cease.

Interface - The interface to the DSVT is conditioned diphase data. The interface to the NCMD is TTL levels.

Performance - Detailed timing and performance characteristics are given in Specification C01-01-02-01A.

3.2.1.2.2 Continuously Variable Slope Delta (CVSD)

The CVSD provides a voice-to-digital converter used to interface analog loops utilizing TA-341 type AC supervised subsets to the NCMD. It allows analog voice subscribers to converse with digitized voice subscribers. Voice digitizing is performed by the compounded delta modulation technique called Continuously Variable Slope Delta Modulation (CVSD). A block diagram of the CVSD is shown in Figure 3-17.

Functional Description - The CVSD technique digitizes voice signals into a single serial digital bit stream. This digital bit stream consists of pulses of fixed amplitude and timing, the only variation being in the pattern of ONEs and ZEROs. When the input level to the CVSD Encoder is increased, more runs of consecutive digits of the same polarity are produced at the digital output. The CVSD Encoder operates by comparing the speech input with the feedback approximation from the Loop Integrator. The output of the Analog Comparator is a logic ONE if the speech input voltage is more positive than the approximation feedback voltage and is logic ZERO if less than the approximation feedback voltage, The output of the Analog Comparator is sampled at the 32 kHz clock rate and three consecutive bits are stored in the three-bit Shift Register. The CVSD Decoder circuit detects whether these three bits are all ONEs or all ZEROs. If they are all ONEs or all ZEROs, a logic ONE is produced at the CVSD Decoder output. The syllabic smoothing Loop Integrator smooths the CVSD Decoder output pulses to produce the control voltage V_c. The Pulse Height Modulator produces a pulse whose amplitude is a linear function of V_c and whose positive or negative sense is a function of the bit stored in the first stage of the three-bit Shift Register. If a ONE is stored in the first

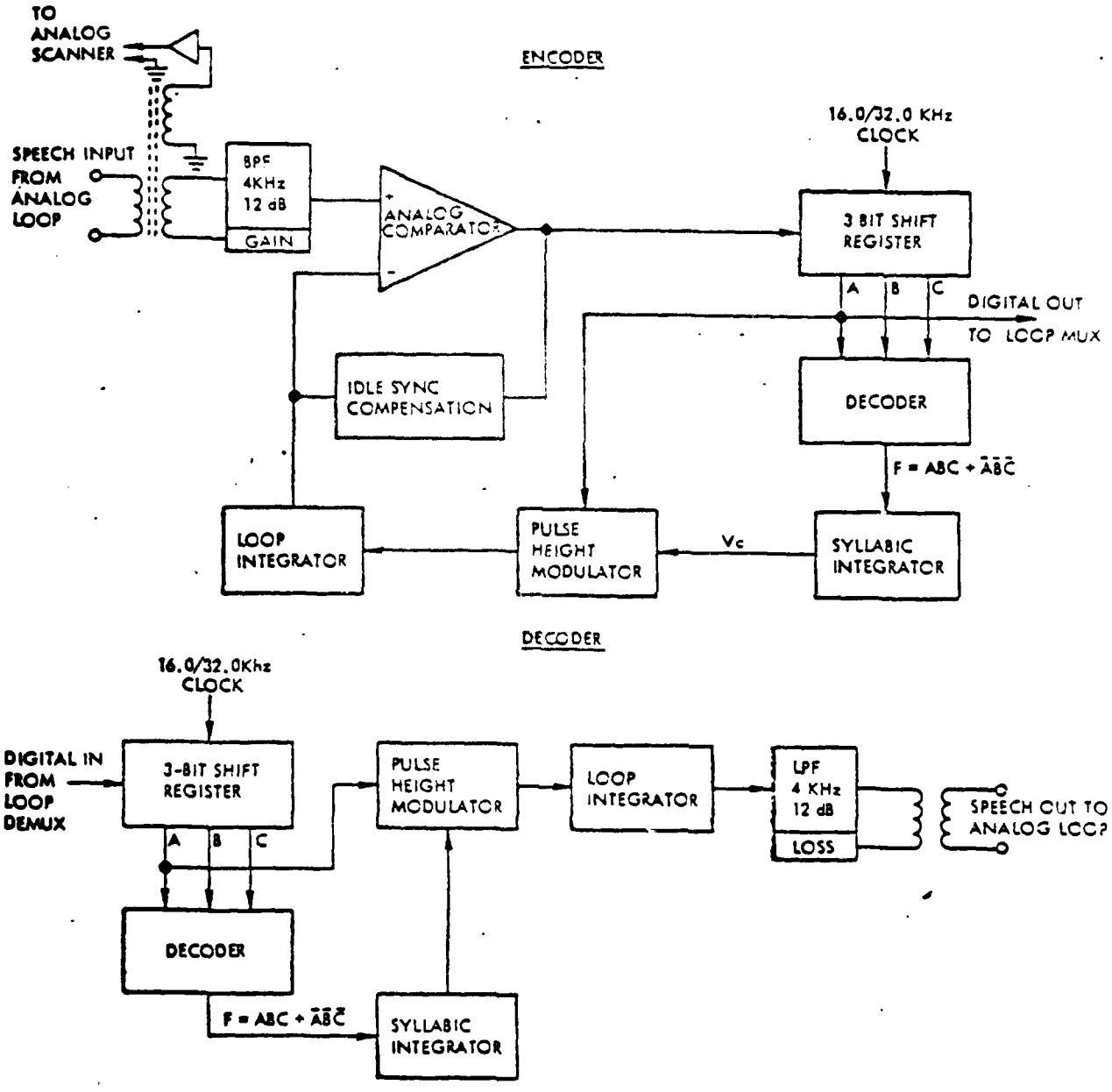


Figure 3-17 CVSD (Analog Loop) Block Diagram

stage, a positive gain is produced by the Pulse Height Modulator, and conversely a negative gain is produced if a ZERO is stored in the first stage of the 33-Bit Shift Register. The Loop Integrator produces the approximated speech input signal by integrating these height-modulated pulses. When no voice signal is present, the output of the CVSD Encoder is forced to be an alternating ONE/ZERO pattern by the idle sync compensation network. As the RMS value of the speech input signal increases, a greater number of runs of three consecutive like digits are produced, which produces more ONEs as the CVSD Decoder output increases. This will increase the peak-to-peak output voltage of the Pulse Height Modulator and will enable the feedback approximation to more accurately follow the input speech signal.

The CVSD Decoder operates identically to the CVSD Encoder with identical characteristics, except that it operates open-loop and does not require the Analog Comparator. A low-pass filter is included at the output of the CVSD Decoder to remove the quantizing noise and other frequency components above 4 kHz.

A gain of +12 dB is provided prior to the CVSD Encoder, with a corresponding attenuation of -12 dB following the CVSD Decoder, to provide level compatibility with digitized voice subscribers such as the DSVT.

Interface - The interface to the Analog Loop is a transformer coupled balanced 600-ohm, four-wire interface. The digital interface to the NCMD and the 32-kHz Clock input are TTL-compatible.

Performance - Detailed performance characteristics are given in Specification C01-01-02-02B.

3.2.1.2.3 Nine Channel Mux/Demux (NCMD)

The NCMD contains a multiplexer and a demultiplexer. The multiplexer combines nine 32-kHz digital data streams into a higher frequency multiplexed data strea. A number of NCMDs may be connected in unison to form a single high-frequency multiplexed digital data stream. The demultiplexer performs the reverse

operation, wherein it separates a multiplexed data stream into nine individual 32-kHz data streams. Several DEMUXs may be used in unison to demultiplex a high-frequency data stream containing more than nine channels into its individual 32-kHz data streams. The modularities and operating frequencies with which the NCMD is compatible are listed in Table 3-4. The table also lists the number of NCMDs that must be used to properly handle the given modularities.

If there are unused channels in a transmission group, the full complement of NCMDs may not be required. In a transmission group with a modularity based on a multiple of nine, one NCMD is required for each block of nine channels sequentially assigned, starting with channel one. In a transmission group with a modularity based on a multiple of eight, one NCMD is required for each block of eight channels.

Function Description - The NCMD consists of a multiplexer, demultiplexer, clock selection logic, selection logic to direct the input and output serial data streams, and fault detection logic, as illustrated in Figure 3-18. Five major functions are performed by this card and are described as follows:

Clock Selection - The clock selection logic shown in the figure determines the rate at which the multiplexing and demultiplexing circuitry operates on the card. Any one of 11 frequencies are selected by manually programming the four plugs labeled F1 through F4. The frequencies that can be selected are those listed in Table 3-5 in the Multiplexed Data Stream Rate column. Table 3-6 lists the binary select fields and the selected clock. The four plugs simultaneously program the 9/8 programmable shift registers used for multiplexing and demultiplexing. The 9/8 programming makes the operation of the card compatible with transmission group modularities based on multiples of 9 or 8.

Multiplexing - The multiplexing logic is represented by register A and the destination selection logic in the figure. The multiplexing

TABLE 3-4 MODULARITIES OF THE NCMD

Number of NC's Required	Demultiplexed Data Stream Rate	Multiplexed Data Stream Modularity	Multiplexed Data Stream Rate
16	32 kHz	144	4.608 MHz
8	32 kHz	72	2.304 MHz
4	32 kHz	36	1.152 MHz
2	32 kHz	18	576 kHz
1	32 kHz	9	288 kHz
15	32 kHz	128	4.096 MHz
8	32 kHz	64	2.048 MHz
6	32 kHz	48	1.536 MHz
4	32 kHz	32	1.024 MHz
2	32 kHz	16	512 kHz
1	32 kHz	8	256 kHz

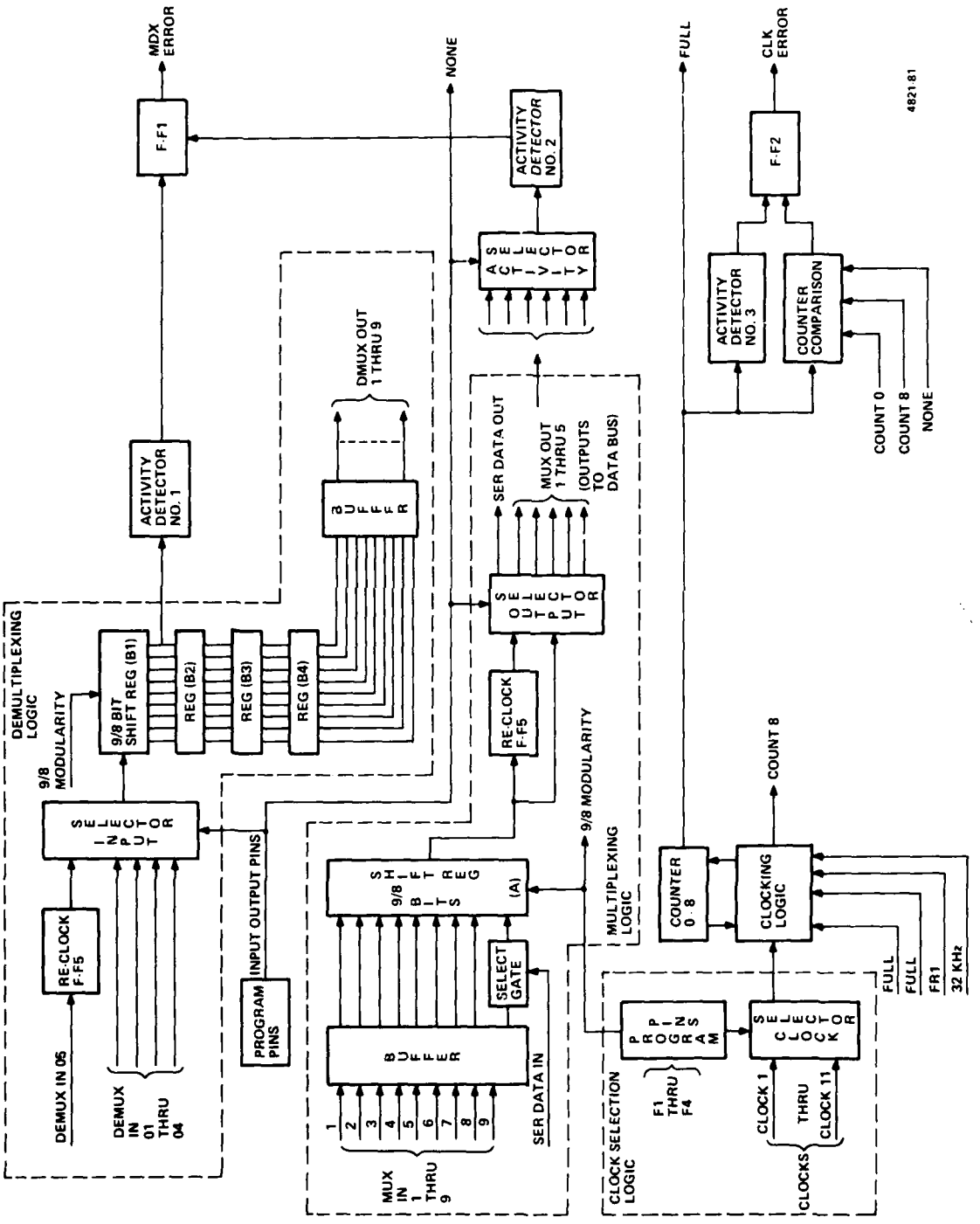


Figure 3-18. NCMD Block Diagram

TABLE 3-5 CLOCK SELECTION BITS

Binary Select Field				Clock Selected
F1	F2	F3	F4	
0	0	0	0	4.608 MHz
1	0	0	0	2.304 MHz
0	1	0	0	1.152 MHz
1	1	0	0	576 kHz
0	0	1	0	288 kHz
1	1	0	1	4.096 MHz
0	0	1	1	2.048 MHz
1	0	1	1	1.536 MHz
0	0	0	1	1.024 MHz
1	0	0	1	512 kHz
0	1	0	1	256 kHz

TABLE 3-6 INPUT OUTPUT SELECTION

Input/Output Programming Plugs					Demux Input Selected	Mux Output Selected
A1	A2	A3	A4	N1		
1	0	0	0	1	DMUX IN 01	MUX OUT 01
0	1	0	0	1	DMUX IN 02	MUX OUT 02
0	0	1	0	1	DMUX IN 03	MUX OUT 03
1	1	1	0	1	DMUX IN 04	MUX OUT 04
0	0	0	1	1	DMUX IN 05	MUX OUT 05
X	X	X	X	0	X	SERDATA

technique uses a parallel in/serial out shift register (Reg A). The framing pulse (FR1) initiates a sequence during which the nine 32 kHz data bits representing the data streams to be multiplexed are loaded into Register A in parallel using a 32-kHz clock and then shifted out in series using the high-frequency multiplexing clock. This serial output is the multiplexed data stream. As shown in Figure 3-19, several NCMD multiplexing sections are connected in series to assemble long streams of data in the modularities listed in Table 3-4. Each of the NCMD multiplexing sections contains logic to select the destination of its serial output. The output may be directed to the next NCMD, or one of the four TGMs or Loop Mux/Demux, as shown in Figure 3-20 Only one output is selected at a time, and when one is selected the other five drivers are turned off, since they use tri-state outputs. The selection is performed by manually programming the jumper plugs labeled A1 through A4 and N1. The jumper labeled N1 identifies which card is the first in a chain of NCMD operations on one trunk. Table 3-6 lists the position for A1 through A4, and N1, along with the selected input/output ports of the NCMD.

Demultiplexing - The demultiplexing logic is represented by registers B1 through B4 and the source selection logic is shown in Figure 3-20. The demultiplexing technique uses serial-in parallel-out shift register B1. The framing pulse F1 initiates a sequence during which nine digital data bits are read in serially into register B1 and then shifted into register B2 in parallel fashion. The nine bits being read in serially represent the high-frequency multiplexed data stream, while the bits placed in B2 represent the demultiplexed 32 kHz digital data bits. The source selection logic selects which of five possible inputs is to be demultiplexed. Several NCMDs are used in unison to demultiplex streams of data in the modularities listed in Table 3-4.

The interconnection of demultiplexers to handle lengthy streams of data bits is shown in Figure 3-20. This operation differs from the interconnection of the multiplexers. The serial data stream in DEMUX No. 1 does not pass through DEMUX No. 2. Each DEMUX has its

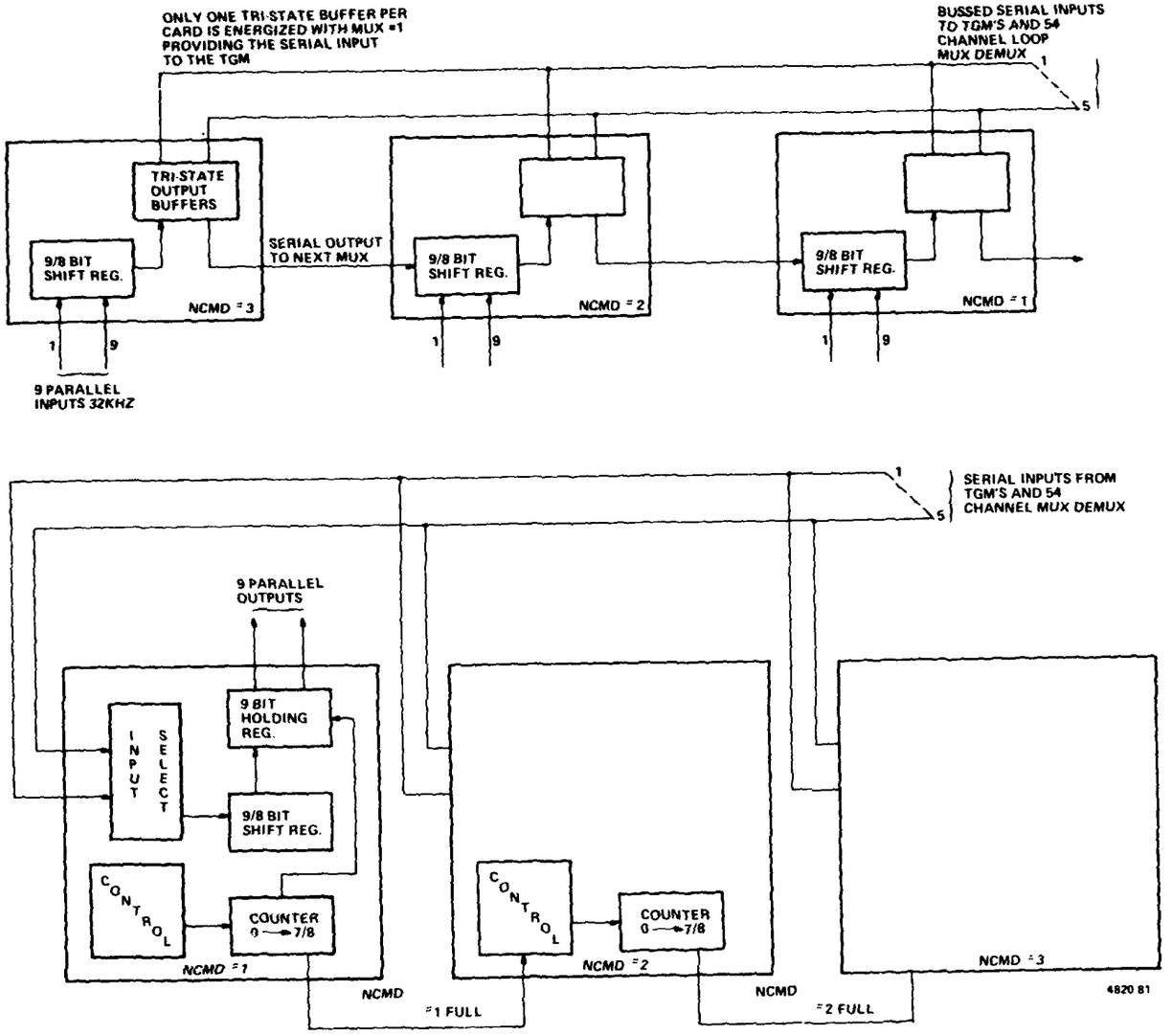


Figure 3-19. Interconnection of Multiplexer Stages

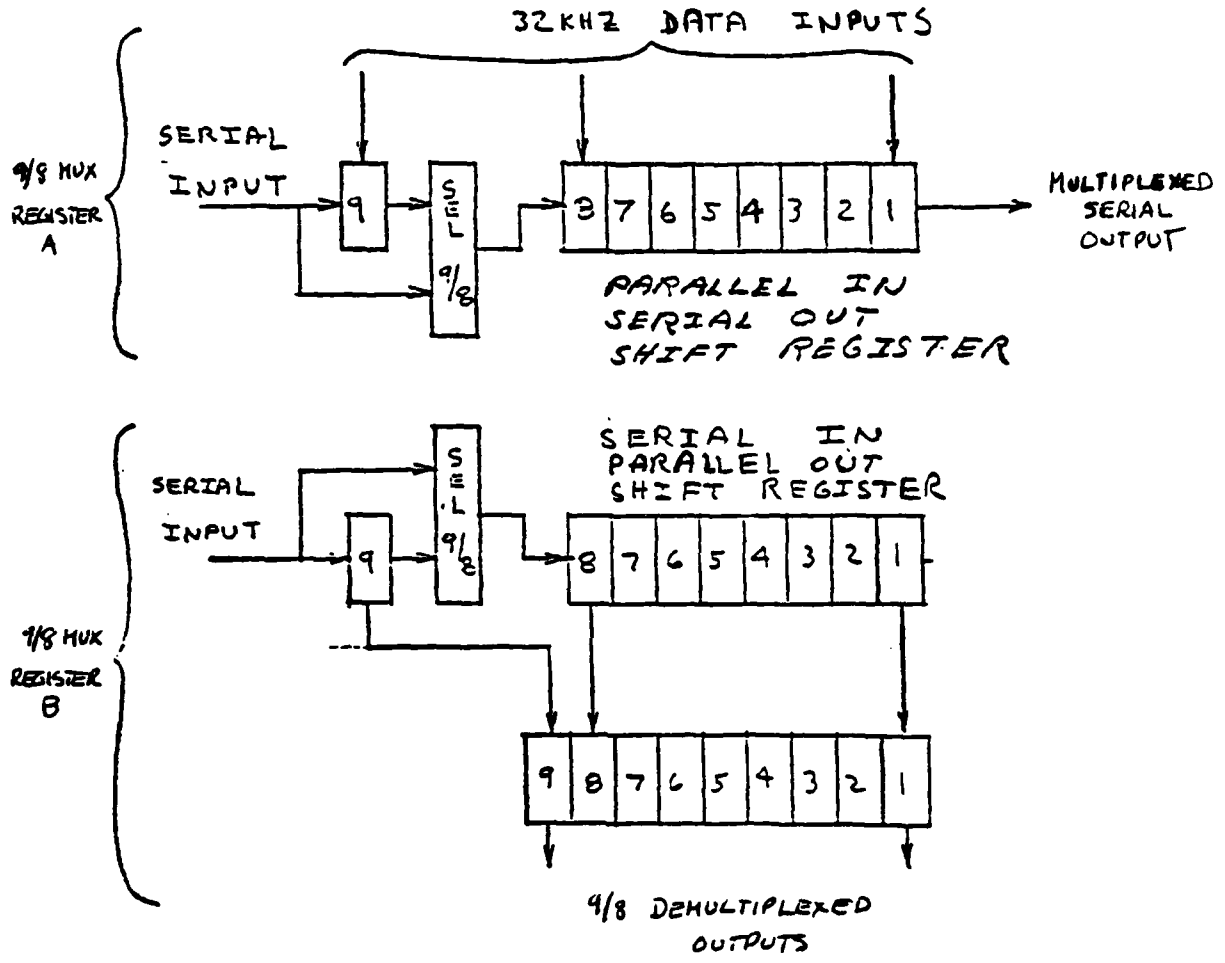


Figure 3-20 MUX/DEMUX 9/8 Operation

own serial input from the selected source. When the framing pulse occurs, DEMUX No. 1 shifts in the serial data while its counter maintains a count of the number of bits being clocked into register B1. After the first 9/8 bits are in B1, these 9/8 bits are shifted in register B1 in a parallel fashion, while DEMUX No. 1 activates the signal line labeled FULL to DEMUX No. 2, which then performs the same operation on the following 9/8 bits. The B2 registers hold the data until the next framing pulse occurs, whereupon they are shifted into register B3. Register B3 is needed to align the data of all DEMUXs, while holding it until the correct transition time of the 32 kHz clock occurs. At that time, the data is clocked into register B4. The DEMUX that is the first in a chain is designated by setting the programming plug N1 to a logic ONE. The proper input to the DEMUX is selected by setting the programming plug A1 through A4. Table 3-6 lists the binary select fields of A1 through A4 and the corresponding input that is selected.

9/8 Conversion - Figure 3-20 shows a diagram of the multiplexer and demultiplexer sections on the NCMD. The four programming plugs F1 through F4 control two select gates which select the ninth bit of the MUX/DEMUX registers for Nx9 modularity operation or bypass it for Nx8 modularity operation. This results in the ninth bit on an NCMD being unused when the modularity of Nx8 is selected. This unused bit does not appear in the output stream, however, since the select gate has bypassed it.

Interfaces - The NCMD is input compatible with the Line Driver/Receiver, the CVSD, and the DLM-A cards on a TTL basis. The output is compatible with other NCMD outputs and the input to the TGM group on a TTL basis. The detail interfaces, timing, and performance are given in Specification C01-01-02-04B.

3.2.1.2.4 Transmission Group Module (TGM)

The Transmission Group Module (TGM) contains two units, the Group Buffer (GB) and Group Framing Unit (GFU). These two units provide for timing adjustment, encryption and decryption, and frame synchronization of digital transmission group data. A block diagram of the TGM is shown in Figure 3-21 .

Functional Description

Group Buffer - The GB receives digital data and data clock from the modem. The data clock rate shall be governed by the clock of each transmitting mode. The daily drift of each switch shall be small enough that the data can be reclocked by means of a small-capacity storage buffer. This buffer shall be organized in a First-In/First-Out (FIFO) manner so that the data will be outputted in the same order as input. It shall be initially set to 50 percent full and, depending on the difference of the two clock rates, shall gradually empty or fill. The buffer shall provide 256 bits (plus or minus 128 bits) of storage for all data rates based on the 32 kb/s loop rate, and 128 bits (plus or minus 64) for those based on the 16 kb/s loop rate. This will allow for a minimum time buffer of plus or minus 27.8 microseconds at the 144 channel group rates. The selection of transmission group modularity shall be effected via manually programmable straps on the TGM cards. Table 3-7 specifies the proper strapping plug arrangements for the various modularities. A separate manual strap shall also be used to select either 16 or 32 kb/s operation of the GB (selection either 128 or 256 bit FIFO size).

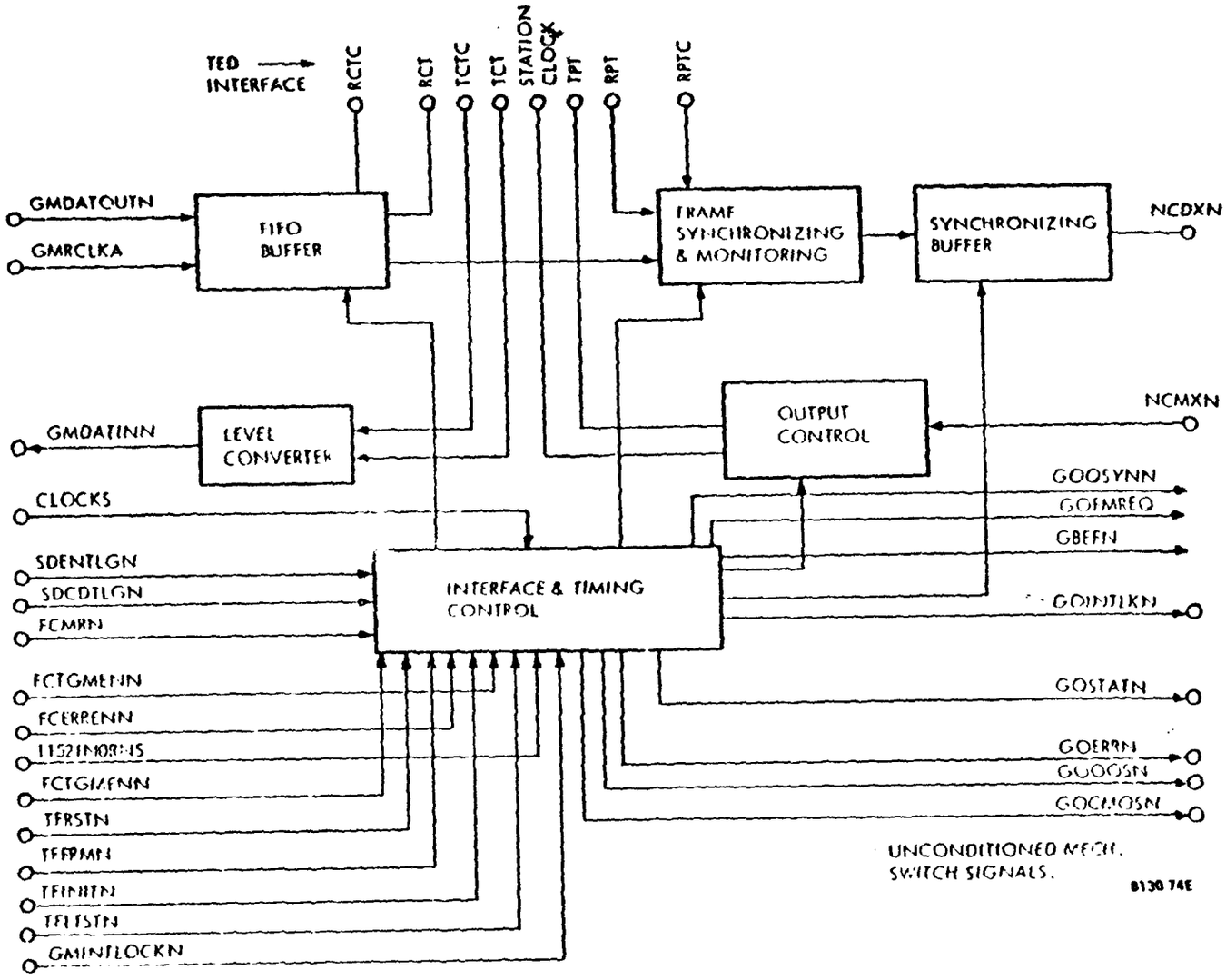


Figure 3-21 TGM Block Diagram

TABLE 3-7 GROUP RATE SELECTION

Channels	Rate (kHz)*	Program Plug Position			
		P0	P1	P2	P3
144	4608	T	1	0	1
72	2304	T	1	0	0
36	1152	T	0	1	1
18	576	T	0	1	0
9	288	T	0	0	1
128	4096	S	1	1	0
64	2048	S	1	0	1
48	1536	S	1	0	0
32	1024	S	0	1	1
16	512	S	0	1	0
8	256	S	0	0	1

*Rate shown for 32 Kb/s Operation

Group Framing Unit - 32/16 kilobits per second (kb/s) channels shall be grouped in 8, 9, 16, 18, 32, 36, 48, 64, 72, 128, or 144 channel groups, which shall each be serviced by a single TGM. The framing information is transmitted on a 4/2 kb/s subchannel. Thus, in a 144-channel transmission group with each channel operating at 32/16 kb/s, there are 1151 bits between successive framing bits in a major frame. During acquisition of framing, only ZEROS plus the framing pulses shall be transmitted on the trunk. The absence of other transmission speeds the search for the frame subchannel. The framing signaling subchannel for a 144-channel trunk is shown in Figure 3-22.

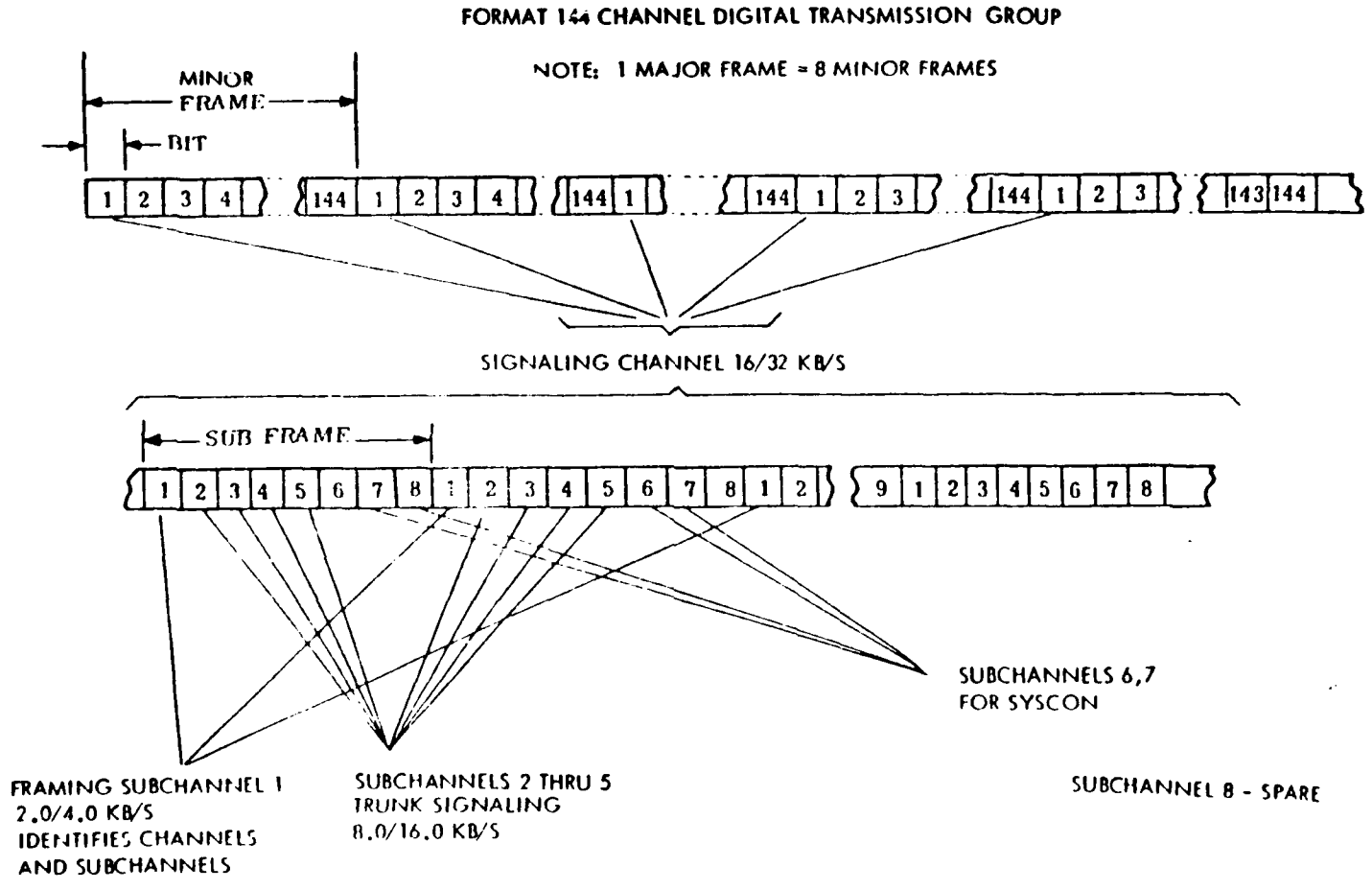


Figure 3-22 Framing Signaling Subchannel

Two distinct framing patterns shall be used to aid in the control of the resynchronization process. The frame pattern transmitted during normal, synchronous operation shall be an alternating ONE-ZERO pattern with traffic on the data channels. During a resynchronization, the TGM shall transmit a framing pattern of all ONES with all data channels set to ZERO. This "frame request" signal shall indicate to the receiving GFU at the other end that a resynchronization is in progress, and it shall respond by removing the traffic from the data channels. Figure 3-20 shows the operational states of the GFU and the use of the two framing patterns.

In the search mode the GFU shall perform a multistage frame acquisition process. During the first level of acquisition, the unit shall search the data stream for the leading one of a prospective frame pattern, and then examine every other suspected frame bit position (skipping the ZEROES of the ONE-ZERO pattern). Successful identification of two correct bits of those examined shall allow the GFU to proceed to the second acquisition level. Once again, every other bit position shall be checked for the presence of a ONE. More than one error in the next three bits examined shall send the unit back to level one. Identification of two our of three bits as correct shall allow progression to level three. At this point, two detectors will be used to examine each of the next 32-bit positions for at least 30 correct bits of either the ONE-ZERO or all ONES framing pattern. If more than two errors are found by both detectors, the unit shall return to level one. Otherwise, the units shall exit the search mode in accordance with the state diagram of Figure 3-23. At the third level, a check shall be made of the data channels to assure that they are ZERO. A separate detector shall be used to examine all data channels for at least 145 ZEROS in 200 bits. Failure to meet this criteria shall send the GFU back to level one. The operation of the GFU search mode is shown in Figure 3-24.

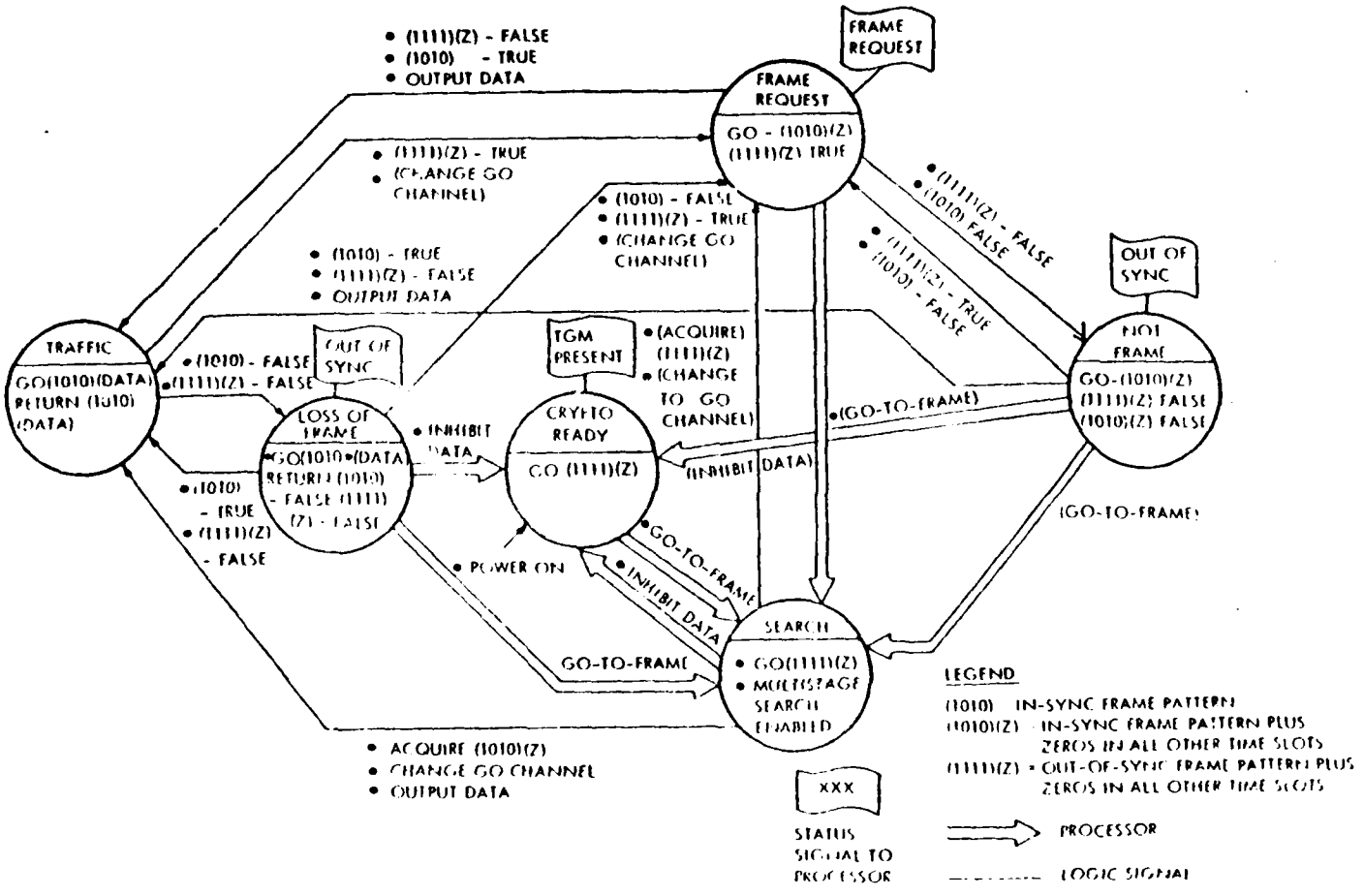


Figure 3-23 GFU State Diagram

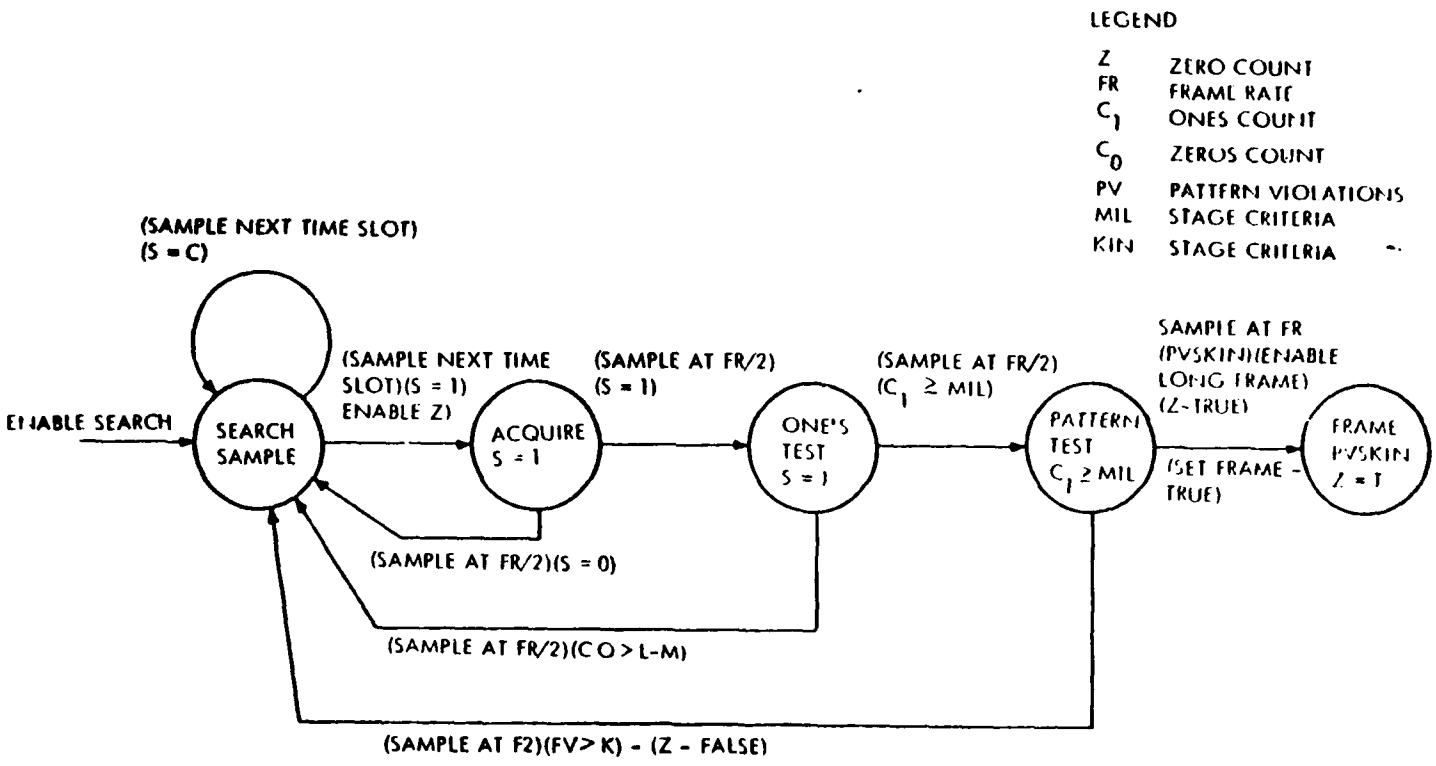


Figure 3-24 Multistage Search

After leaving the search mode, the GFU shall continue to monitor the frame pattern using a 75/128 criterion to identify the ONE-ZERO pattern and a 30/32 criterion in conjunction with the ZEROS detector to identify the all-ONES pattern. The acceptance criteria for all levels of search and monitoring are specified in Table 3-8.

TABLE 3-8. SEARCH AND MONITORING ACCEPTANCE CRITERIA

Function	Frame/Data Pattern	Event - True
Multistage Search	(1010)	2:2 2:3 30:32
Multistage Search	(1111)	(Same)
Monitor	(1111)	30:32
Monitor	(1010)	75:128
Zeros Monitor	(Z)	145:200

The output control of the TGM shall effect the data inhibits and frame pattern changes as shown in Figure 3-23. The TGM shall be responsible for replacing the 1100 subchannel framing pattern inserted in the channel 1 frame position by the Trunk Signaling Buffer (TSB) with the appropriate main channel framing pattern.

Synchronizing Buffer. The GFU shall be responsible for the synchronization of the incoming data to the system framing reference. It shall do this in such a manner as to always present the framing subchannel or channels on the same output channel of th Trunk Signaling Buffer Demultiplexer. During the out-of-s ite, data to the group multiplexer shall be inhibited in the all state.

Manual synchronizing inputs shall allow for three-step manual activation of selected TGM commands. If the INITIATE plus the RESET lines are activated, it shall reset the buffer and permit only the framing code to be outputted. If the INITIATE plus the FRAME lines are activated, it shall initiate a frame sync search. With the manual switch in the OPERATE position, all other manual inputs shall be disabled.

Manual controls, such as those described above, are included on the edge of the RCHYB card for the manual synchronization process. Examination of the state diagram of Figure 3-23 indicates that this card group requires a small logic cluster to simulate processor sync-status message pickup, decision, and command back to TGM. This logic is included on the RCHYB PCB.

Interface - All signals, with the exception of those usually associated with TED interfaces (not applicable to fiber optics application), are TTL standard logic levels.

Performance - Detail interface line definitions and timing are described in Specification C01-01-02-05B.

3.2.1.2.5 Diphase Group Modem (DGM)

The diphase group modem transmits and receives data and provides baseband/diphase conversion as well as clock extraction and insertion functions. The modem operates with group sizes of 8, 9, 16, 18, 32, 36, 48, 64, and 72 channels. For 32 kb/s channels, the trunk transmission rates are 256, 288, 512, 576, 1024, 1152, 1536, 2048, and 2304 kb/s. The DGM functions as shown in Figure 3-25.

The DGM provides two major functions: Modulator and Demodulator.

Modulator - The modem modulator consists of the data modulator, line driver, and transformer and modulates the input baseband data stream. The digital data is conditioned (differentially encoded), diphase-modulated by the data modulator, and applied to coaxial cable by means of a line driver. Since the fiber-optic application interface requirement to and from the Optic Modem card is TTL, some of the above line driving circuitry will be removed from the card. A rate selector selects the required clock frequencies for the specified data rate. Straps are used to generate the code required for the particular rate desired.

Demodulator - The demodulator consists of an input transformer, attenuator selector, equalizer, hard limiter, clock recovery circuit, carrier detector, and data demodulator. Three or four of these circuits will be removed since the interface to optic modem is TTL. The modem demodulator extracts both baseband data and a bit synchronous clock from the input diphase modulated signal. The input diphase signal is transformer-coupled to the demodulator input where a line equalizer compensates for line-induced signal distortions.

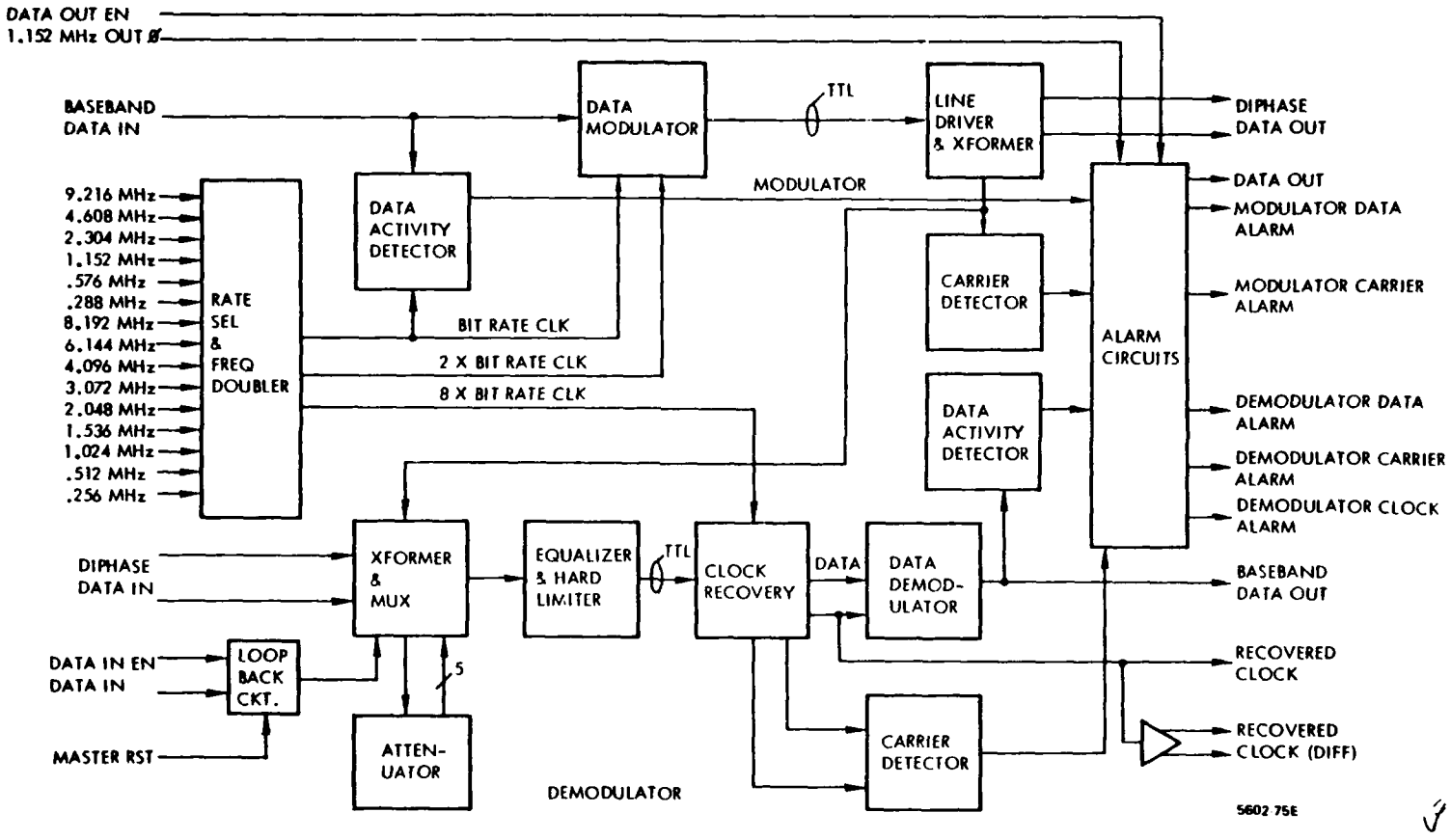


Figure 3-25. Diphase Group Modem Block Diagram

The clock recovery circuit includes a phase-locked-loop and derives the recovered clock from the diphase data. The data decoder differentially decodes the sampled diphase signal and outputs demodulated baseband data and the recovered clock.

Interface - The interface on both sides of the DGM is TTL logic levels.

Performance - Detailed performance characteristics are given in Specification C01-01-02-03A.

3.2.1.2.6 Local Timing Generator (LTG)

The local timing generator does not have a Critical Item Specification as do the other TTC-39 cards being used for the C&S link operation. The function of this card can best be described as a large frequency-divider operation which derives all of the local timing needed by cards in group. Two clocks on the RDHYB cards provide the LTG with the required 18.432- and 16.384-MHz squarewaves (TTL). The LTG provides output clocks of the following frequencies:

	8.192MHz	3.072MHz
	4.096MHz	1.536MHz
9.216MHz	2.048MHz	153.6kHz
4.608MHz	1.024MHz	38.4kHz
2.304MHz	512kHz	19.2kHz
1.152MHz	256kHz	
576kHz	64kHz	
288kHz	32kHz	
	4kHz	
	2kHz	

A subset of these frequencies are being used in the fiber-optic C&S application.

3.2.1.2.7 Line Driver/Receiver Card (LNDR)

The LNDR card contains standard TTC-39 driver and receiver circuits collected together on a single PCB for the fiber-optic application. These circuits fulfill the requirements of interfacing NCMD input and output levels (TTL) with the various Alarm, Select, Status, and TTY lines. Refer to Figures 3-26 through 3-31 for the circuit configuration used.

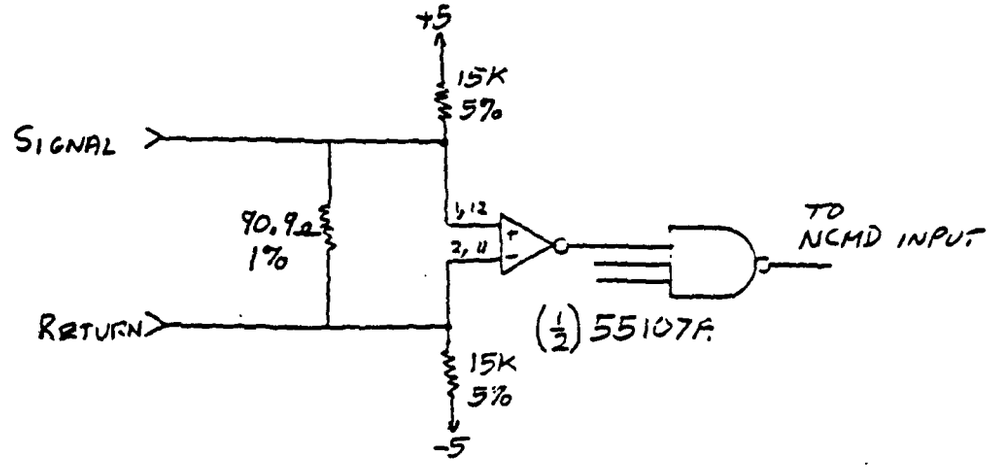


Figure 3-26 Line Receiver - Type R1

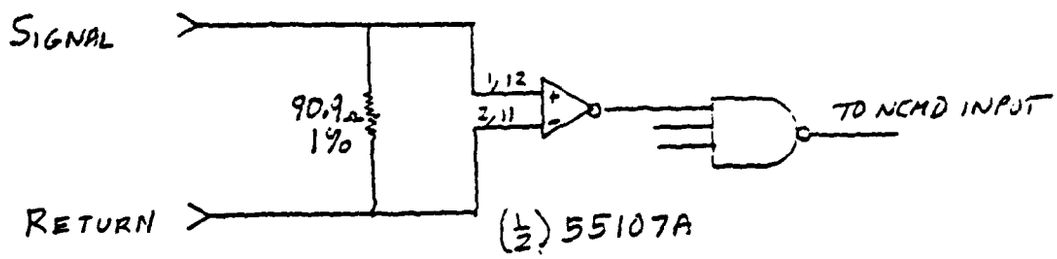


Figure 3-27 Line Receiver - Type R2

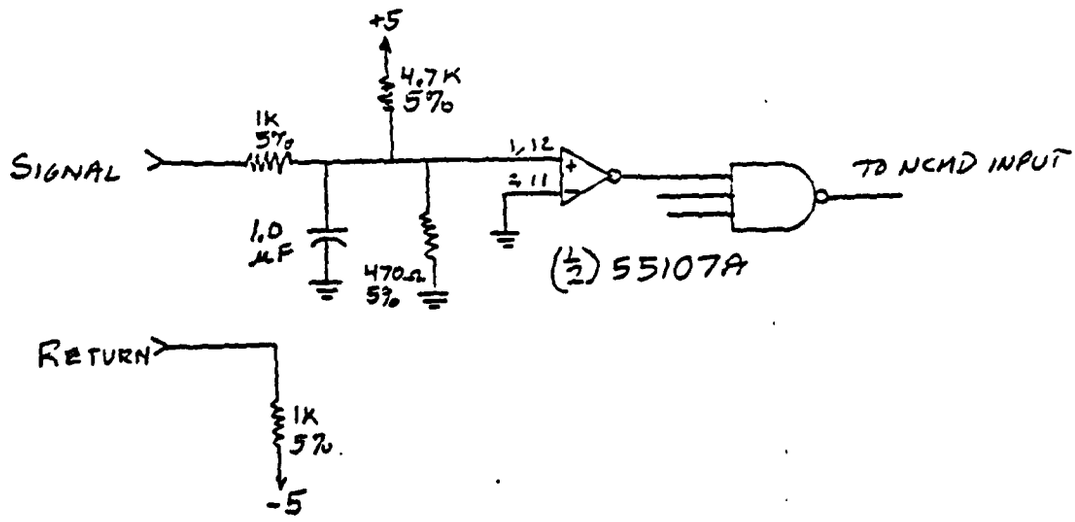


Figure 3-28 Line Receiver - Type R3

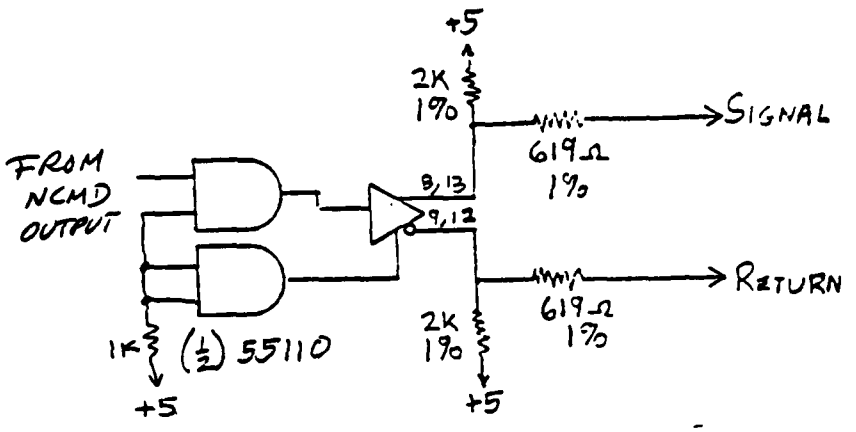


Figure 3-29 Line Driver - Type D1

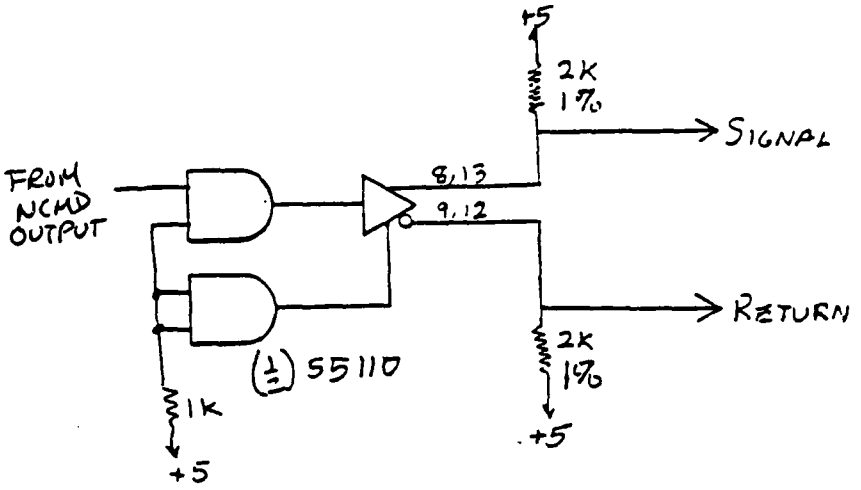


Figure 3-30 Line Driver - Type D2

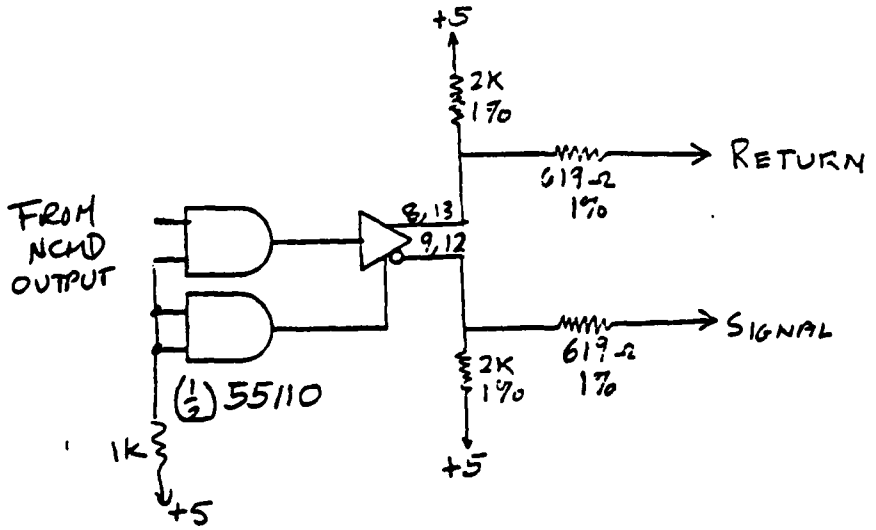


Figure 3-31 Line Driver - Type D3

3.2.1.2.8 Resistor/Clock/Hybrid Card (RCHYB)

The RCHYB card is the catch-all card that picks up miscellaneous circuits not already covered by the selection of standard TTC-39 cards in the fiber-optic nest. The card contains terminating resistors of 91 ohms, for the lines that interface with the IOX signals at the CIC cards, and an oscillator to supply the required 16.384 or 18.432 MHz inputs to the LTG card. This circuit is taken from the design used on the CIC17 Message Processing Interface PCD SM-E-809540. Lastly, there is a circuit to perform 2 to 4-wire conversion and power reconstruction at both ends of the fiber-optic link, including a direction controller to manage a half-duplex operation. In the case of both the clock and the intercom, two circuits are required, so that there are two cards of this type in the nest.

The intercom hybrid circuit converts an intercom output to one suitable for input to a CVSD card, so that the intercom signal can be transmitted over a fiber optic path. The intercom hybrid circuit converts the output of a CVSD card to one suitable for input to an intercom. The above conversions involve performing the following two functions:

a. Convert from 2-wire to 4-wire from the intercom to the CVSD card, and from 4-wire to 2-wire from the CVSD card to the intercom.
b. Reduce the signal level output by the intercom to one appropriate for the CVSD card, and increase the signal level output by the CVSD card to one appropriate for the intercom.

Circuit Description

The intercom hybrid circuit has four basic circuit elements:

1. Transmitter to CVSD card
2. Receiver from CVSD card
3. Voice signal level detector
4. Control logic.

1. Transmitter to CVSD Card - The 4W maximum output of the intercom must be converted to the -2 dBm maximum input of the CVSD card.

   -2 dBm = .631 mW

   4W into 10 ohms = 6.32 V_{rms} signal level

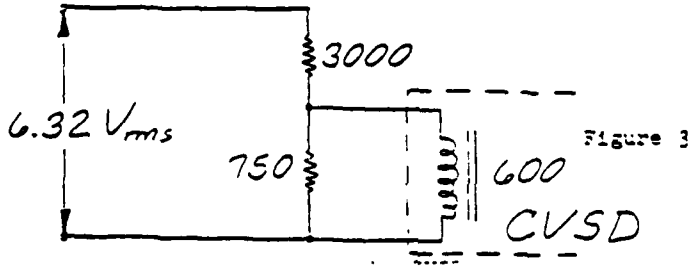


Figure 3

This circuit presents the CVSD input with 600 ohms (3000 || 750) and also delivers .66 mW to the CVSD input.

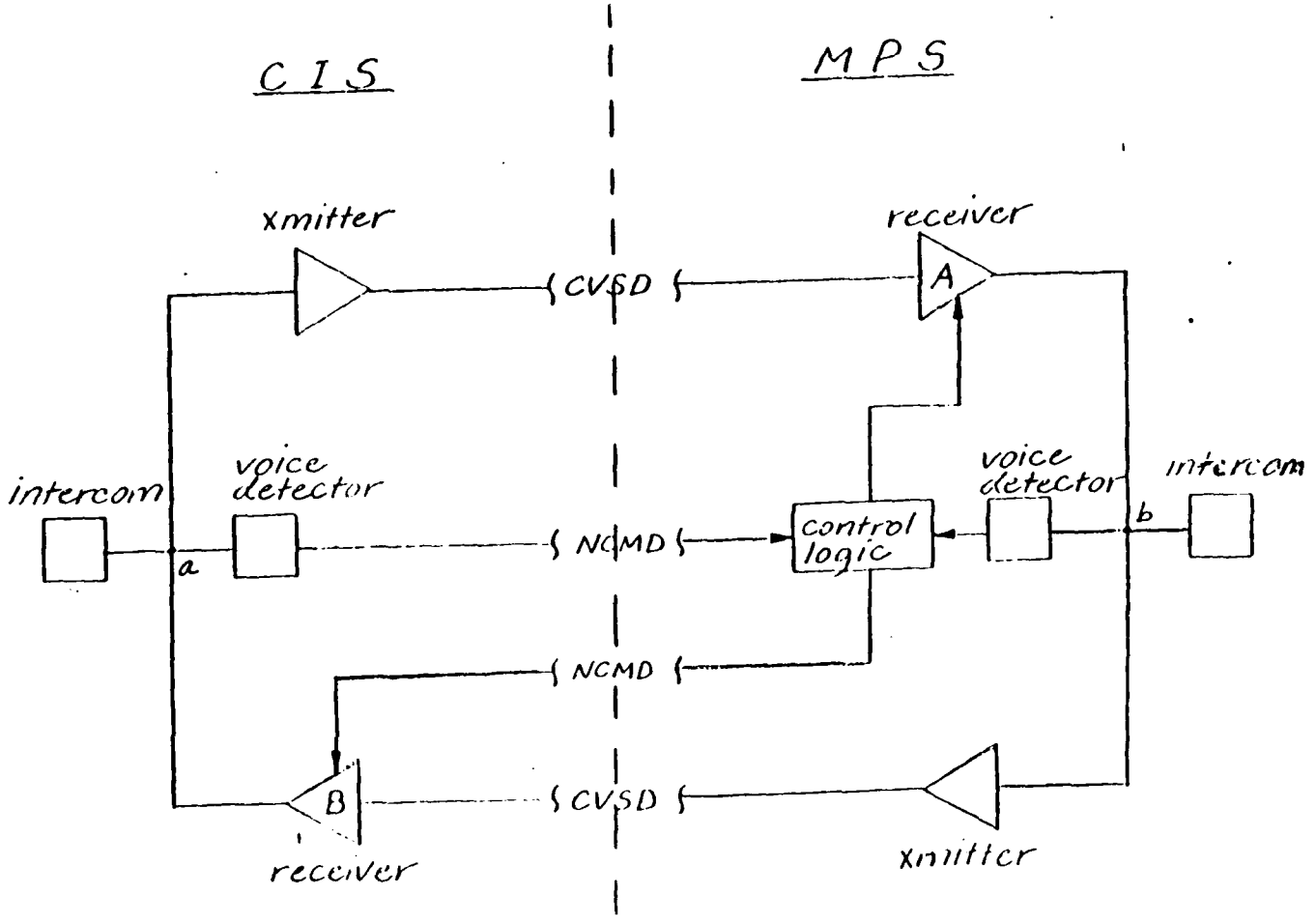


Figure 3-32 Resistor/Clock/Hybrid Card Block Diagram

The receiver presents the CVSD output with 600 ohms. Assuming that the CVSD card can deliver .63mW to it, then the voltage across this resistor will be $.62V_{rms}$.

$$\text{Gain} = \frac{8200 + 1000}{1000}$$

$$= 9.2$$

$$\text{SO } V_{orms} = 5.7\ V_{rms} = 8.1\ V_{peak}$$

The transformer coupling this signal back to the intercom has:

$$\frac{Z_1}{Z_2} = \frac{10}{16} = .625 \text{ impedance ratio}$$

$$\frac{N_1}{N_2} = \sqrt{\frac{10}{16}} = .791 \text{ turns ratio}$$

Referring everything to the secondary side of the transformer:

(.27) (1.6) + .7 (transformer resistances)

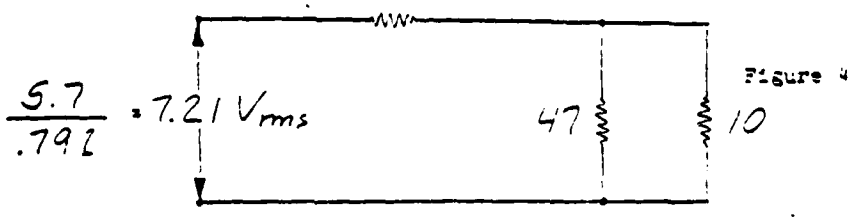
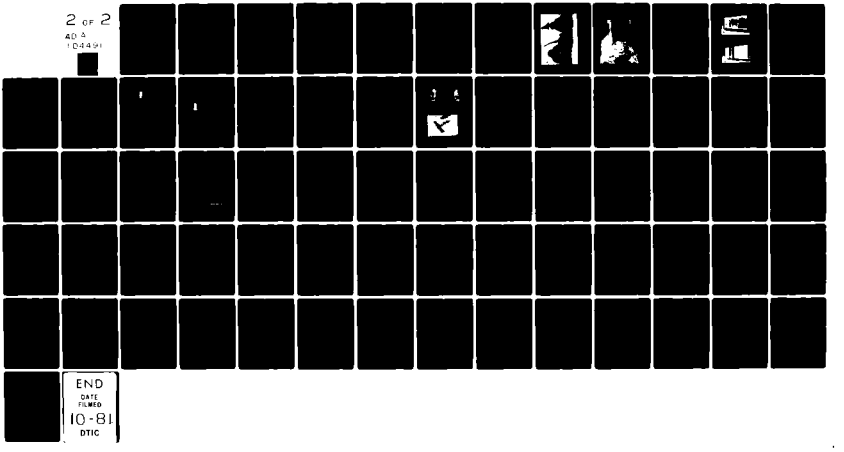


Figure 4

This arrangement will deliver 4W to the 10-ohm load.

AD-A104 491 GTE PRODUCTS CORP NEEDHAM HEIGHTS MA COMMUNICATION S--ETC F/G 17/2
LOCAL DISTRIBUTION FIBER OPTIC CABLE COMMUNICATION SYSTEM.(U)
MAR 81 J SPLAINE, F J SAVELL DAAK80-79-C-0508
UNCLASSIFIED CORADCOM-79-0508-F NL

2 OF 2
AD A
104491



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DATE FILMED
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3. Voice Signal Level Detector - The voice signals are coupled through a 1:1 transformer into a rectifier with a long RC time constant (1.6 seconds). The time constant is long in order to allow the user to pause briefly (1 or 2 seconds) between words without losing control of the transmission path. The rectifier output is fed into a voltage divider and then a comparator to determine whether voice signals are present on the line or not. The voice threshold level was determined using the following ratio:

$$\frac{4W}{.631mW} = \frac{x}{.126mW\ (-9\ dBm)}$$

$$x = .8W$$

.8W into 10-ohm load yields

2.83 V_{rms} = 4 V_{peak} signal

The voltage divider and diode are to protect the comparator from too large signal swings. the 4 V_{peak} signal will be rectified and divided down:

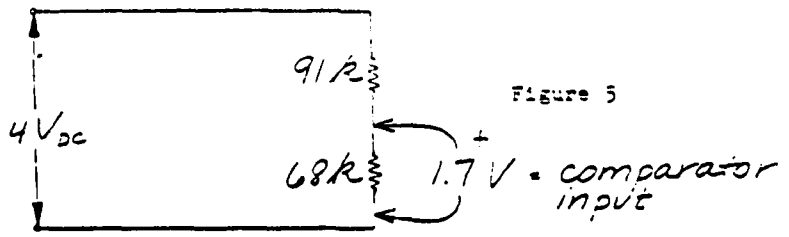


Figure 5

Thus the voice threshold level was set to 1.0V, which is low enough to detect this minimum even when it is allowed to decay for a second. The output of the comparator is TTL compatible.

4. Control Logic - The control logic accepts inputs from each of two voice-level detectors and outputs TTL signals that control two SPDT analog switches. The state table used in designing the control circuit is shown below. A NOR gate was added at the output of the control logic to ensure that both receiver paths are never closed at the same time. In the event that both intercoms start to talk at the same time, control is thrown to path B.

   A complete schematic of the resistor/clock/hybrid card is shown in Figures 3-33 and 3-34 . A power dissipation estimate is shown in Table 3-9.

STATE TABLE:

Present State	ab 00	01	11	10
AB				
00	00	01	01	10
01	00	01	01	01
11	ØØ	ØØ	ØØ	ØØ
10	00	10	10	10

0 = path open
1 = path completed

3.2.2 Optical Modems

The same modem design has been used for both the MPS and the CIS shelters. For a description see Section 3.1.2.

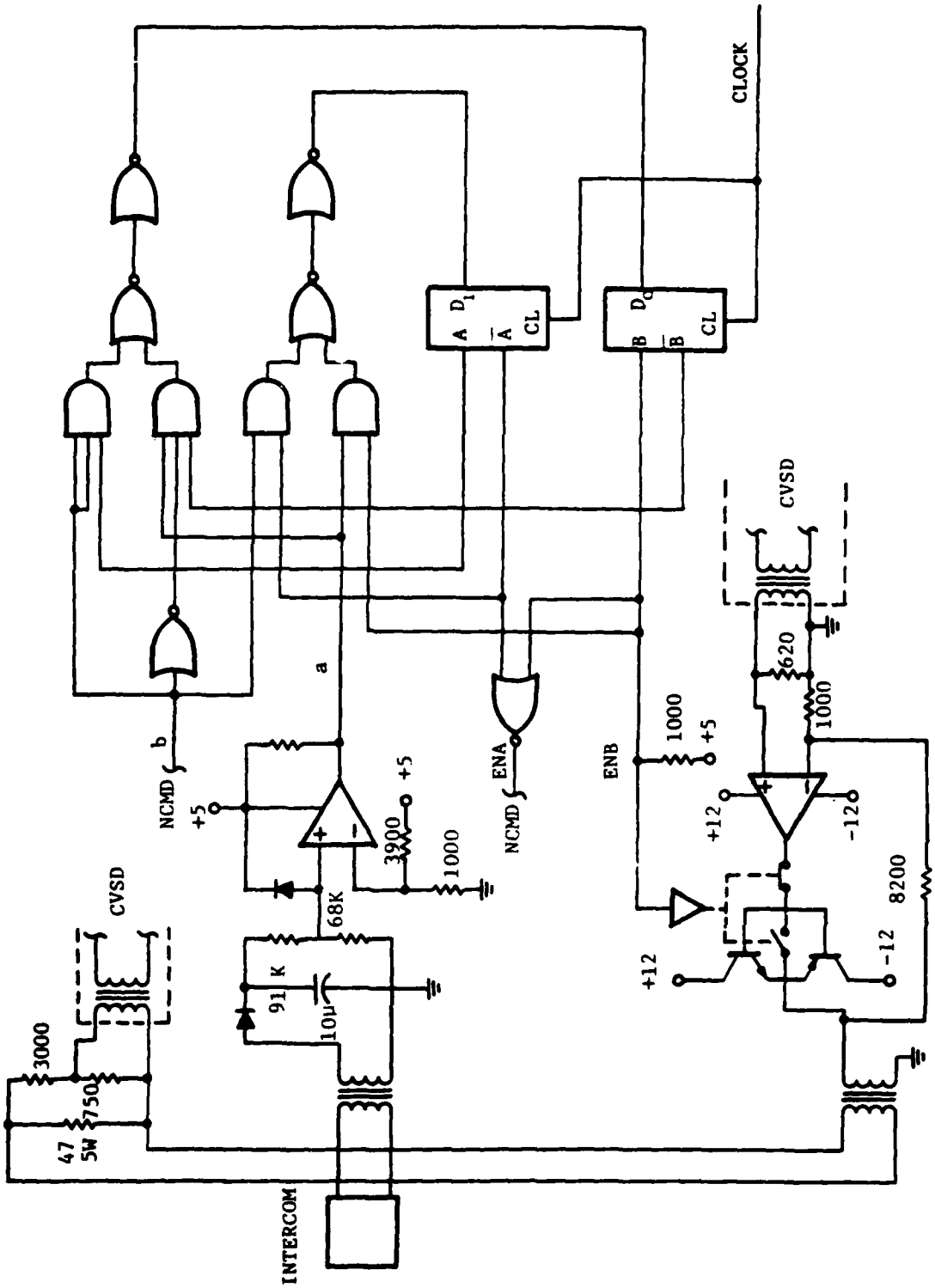
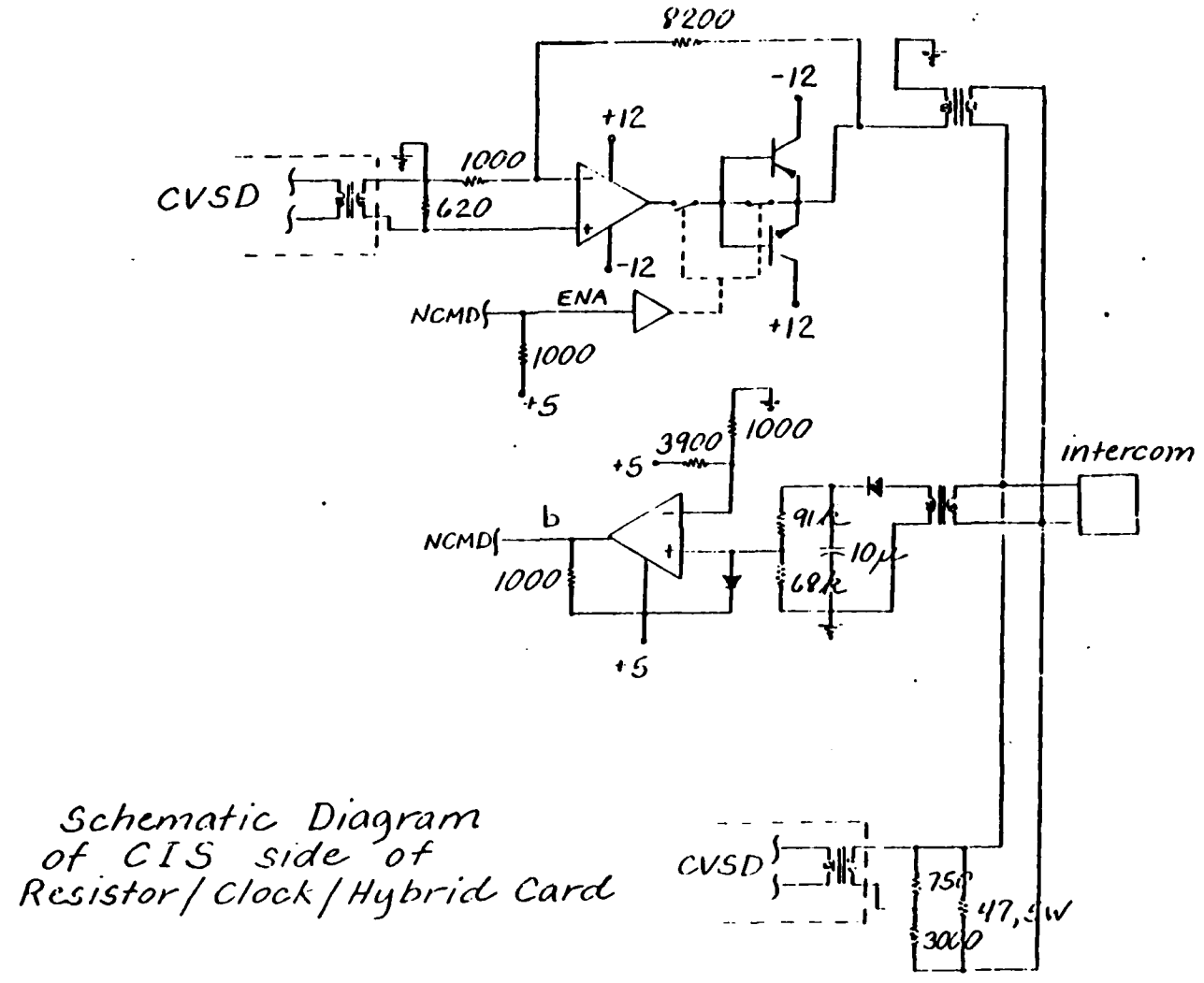


Figure 3-33. Schematic Diagram, MPS Side of Resistor/Clock/Hybrid Card



Schematic Diagram
of CIS side of
Resistor/Clock/Hybrid Card

Figure 3-34. Schematic Diagram - CIS Side of Resistor/Clock/Hybrid Card

TABLE 3-9. HYBRID CARD POWER DISSIPATION ESTIMATE

Component	Power Dissipation	Watts
+5 V Power Supply		
LM111:	.03	x2 = .06
V. Divider:	.005	x2 = .01
1000-ohm res:	.025	x2 = .05
Pullups:	.025	x2 = .05
Switch:	.0015	x1 = .0015
NOR:	.027	x1 = .027
AND:	.033	x1 = .033
Flipflop:	.04	x1 = .04
Total = 270 mW		.27
+12 V Power Supply		
747:	.067	x1 = .067
Feedback:	.0036	x2 = .007
Switch	.0072	x1 = .007
Transistors:	5.0	x2 = 10.0
Intercom, etc:	4.8	x2 = 9.6
Transformer:	.67	x2 = 1.34
Total = 21 W		21.0

3.3 Physical Implementation

3.3.1 Optical System Inter and Intra Shelter Connection

Figure 3-35 shows schematically the Optical System Interconnections. There are two of these cable and connector assemblies per AN/TYC-39 System.

The external cable assembly consists of 100 feet of six fiber cable developed by ITT for CORADCOM and covered by CORADCOM Specification EL-55-0198-001A Appendix A, 7 March 1978 with Hughes six channel optical connectors (sealed contacts and strain relief) on each end. These are hermaphroditic connectors Hughes Part No. 1127029S (see Figure 3-36).

A physical comparison of the new optical intershelter cables and the existing metallic cables is shown in a photograph (Figure 3-37) showing the connection to the actual shelter.

3.3.2 Nest Design

The card nest is a single-row multi-card nest as schematically shown in Figure 3-38; it weighs 42 pounds and is 19 inches wide by 9 inches high be 15 inches deep. Printed Circuit Cards are inserted and extracted from the front. (See shelter installation Figures 3-39 and 3-40.) A nest cover which is attached to the nest mounting frame, keeps the cards in position during the operational and transport modes. The nest is made from 6061-T6 wrought aluminum alloy. Card guides made from beryllium copper are spaced on 0.4-inch centers and provide a good mechanical retention system and thermal path for heat generated on the card to the card nest.

Electrical input/output connections are made on an input/output connector plate located at the rear of the nest (see Figure 3-38). Four 66-pin connectors are provided. From the input/output connectors, wires are brought to a multipin wire wrap motherboard where the interconnections between printed circuit cards are made. Gas-tight electrical wirewrap connections are made on the motherboard.

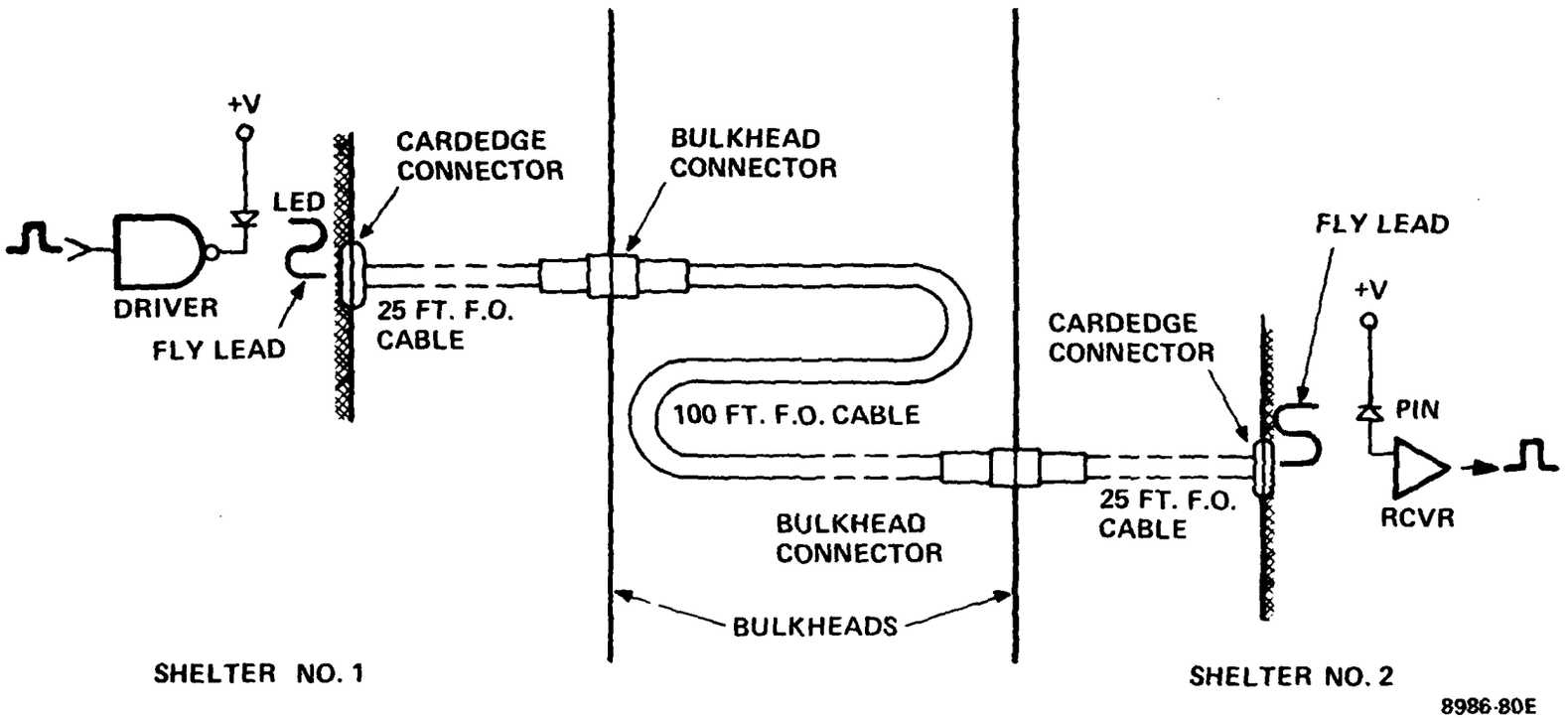
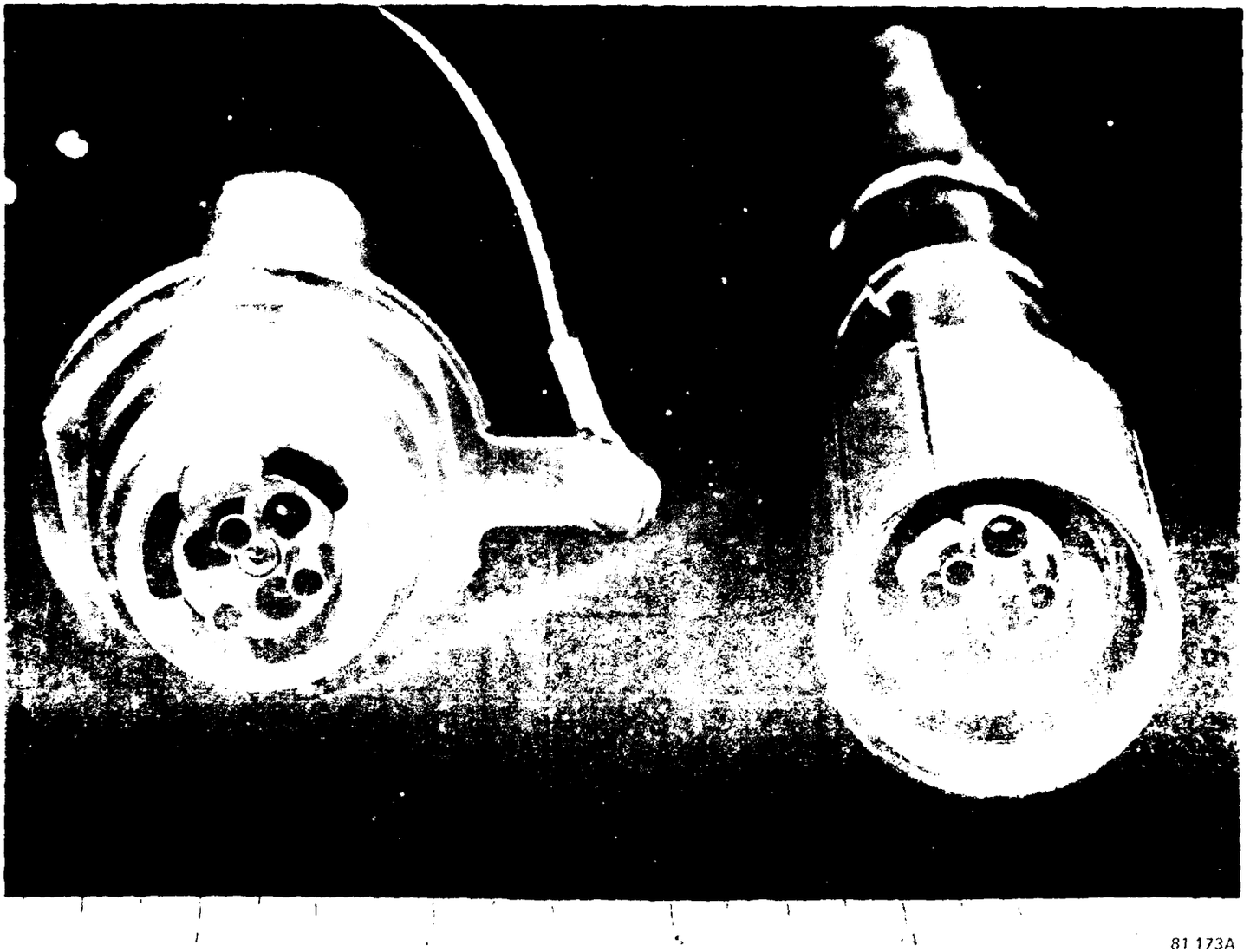


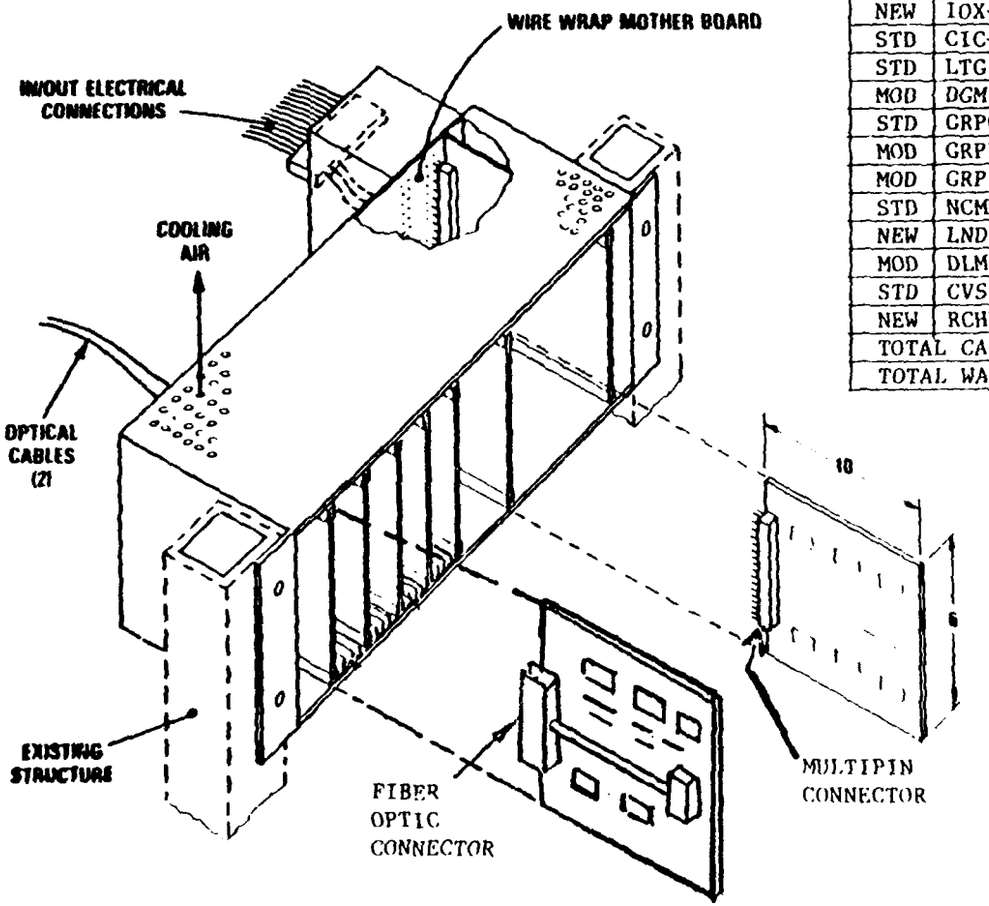
Figure 3-35. Fiber Optic Cable with Connectors



81 173A
4576 81

Figure 3-36. Hermaphroditic Connectors

Figure 3-37. Fiber Optic Interconnect Cables (above) Shown with Replaced Electric Cables (below)



DES	TYPE	MPS	CIS	POWER
NEW	OPTO/XR	2	2	3.13
NEW	IOX-R	2	2	13.20
NEW	IOX-T	2	2	9.72
STD	CIC-2	2	4	3.40
STD	LTG	1	1	12.20
MOD	DGM	1	1	6.50
STD	GRPOT	1	1	13.50
MOD	GRPBF	1	1	13.50
MOD	GRPFR	1	1	13.50
STD	NCMD	3	3	3.00
NEW	LNDR	1	1	3.30
MOD	DLM	1	1	2.85
STD	CVSD	2	2	1.53
NEW	RCHYB	2	2	11.02
TOTAL CARDS		22	24	
TOTAL WATTS		108	115	MAX
		65	69	AVG

Figure 3-38 LDFOCCS Nest

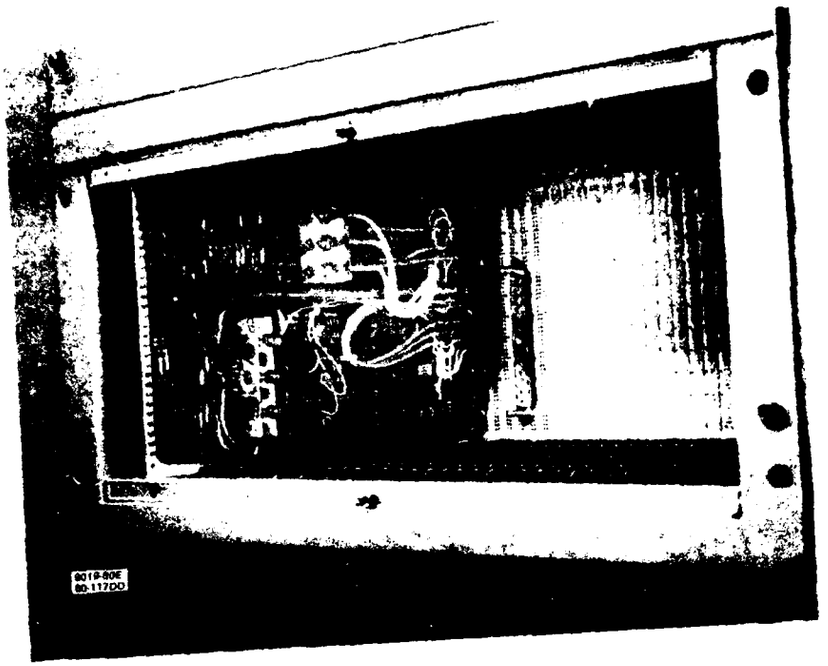


Figure 3-39. Optical Modem in Standard AN/TYC-39 Equipment Nest

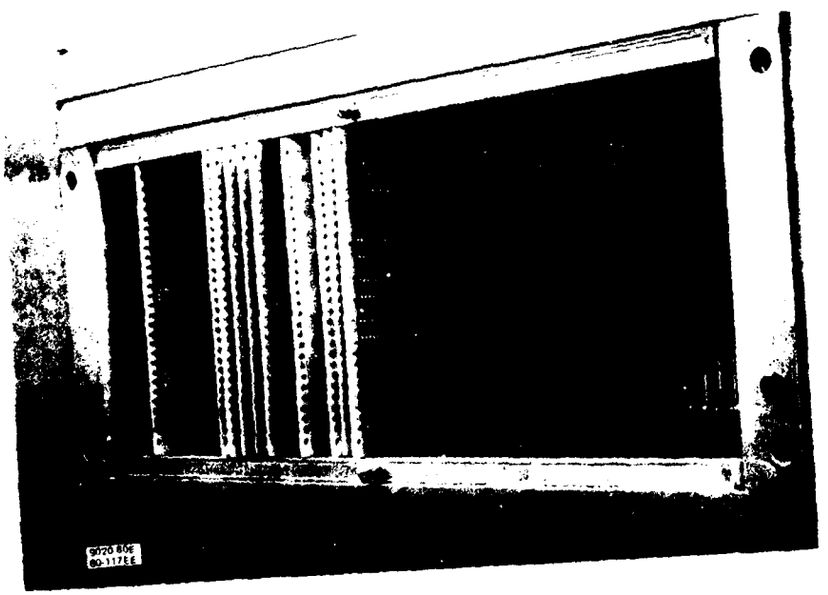


Figure 3-40. Optical Cards Compatible with Standard AN/TYC-39 Cards

The optical cables come into the nest directly via two input optical connectors located on the wire wrap motherboard. Strain relief is built into the optical connector to prevent inadvertent damage to the optical cables.

The nest is mounted on aluminum angle support rails which are tied to the main support structure. Rails are also provided above the nest to preclude the nest from vibrating should loads be applied in a vertical direction as, for example, when the shelter is dropped.

An aluminum front cover is positioned over the front of the nest to keep the cards in position during transport modes.

There are 22 cards in the MPS shelter and 24 cards in the CIS shelter. The cards are arranged in these nests as shown in Figures 3-41 and 3-42.

3.3.3 Nest Mounting Locations

The LDFOCCS nest location in the MPS shelter is shown in Figure 3-43. Specifically, the nest replaces the Tape Drawer, SM-D-811157, at the rear roadside corner of the shelter. Mounting rails are added to the main support structure to provide support for the optic nest. Approximately two inches of space is provided between the LDFOCCS nest and the storage drawer above it, so that air coming from the nest will not be presented with too great a pressure head.

The LDFOCCS nest location in the CIS shelter is shown in Figure 3-44. Specifically, the nest replaces the storage compartment Drawer Assembly, SM-D-813602, at the center of the roadside racks in the shelter. Aluminum support rails are added to the existing structure to provide support for the nest.

3.3.4 Printed Wiring Board Descriptions

All LDFOCCS Printed Wiring Boards (PWB) meet the AN/TTC-39 Criteria Specification SM-A-810507. PWB dimensions are $\pm$0.01 inch. Board thickness will be 0.075 inch maximum. Overall height of the PWB assembly are 0.750 inch maximum with the exception of the optic cards in which the maximum height shall be 1.14 inch. Maximum weights of the boards will be 1.0 pound.

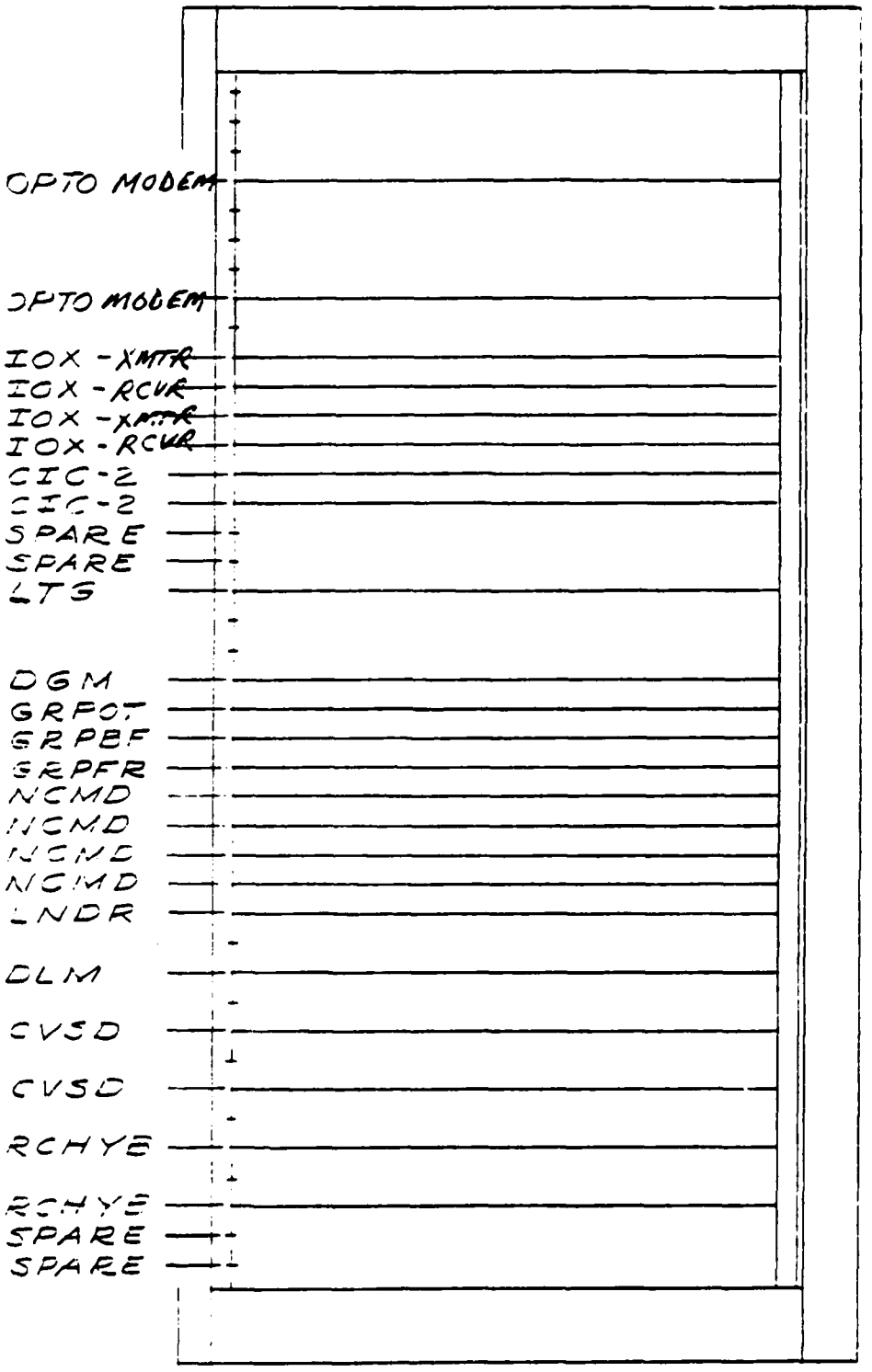


Figure 3-41 MPS Card Arrangement

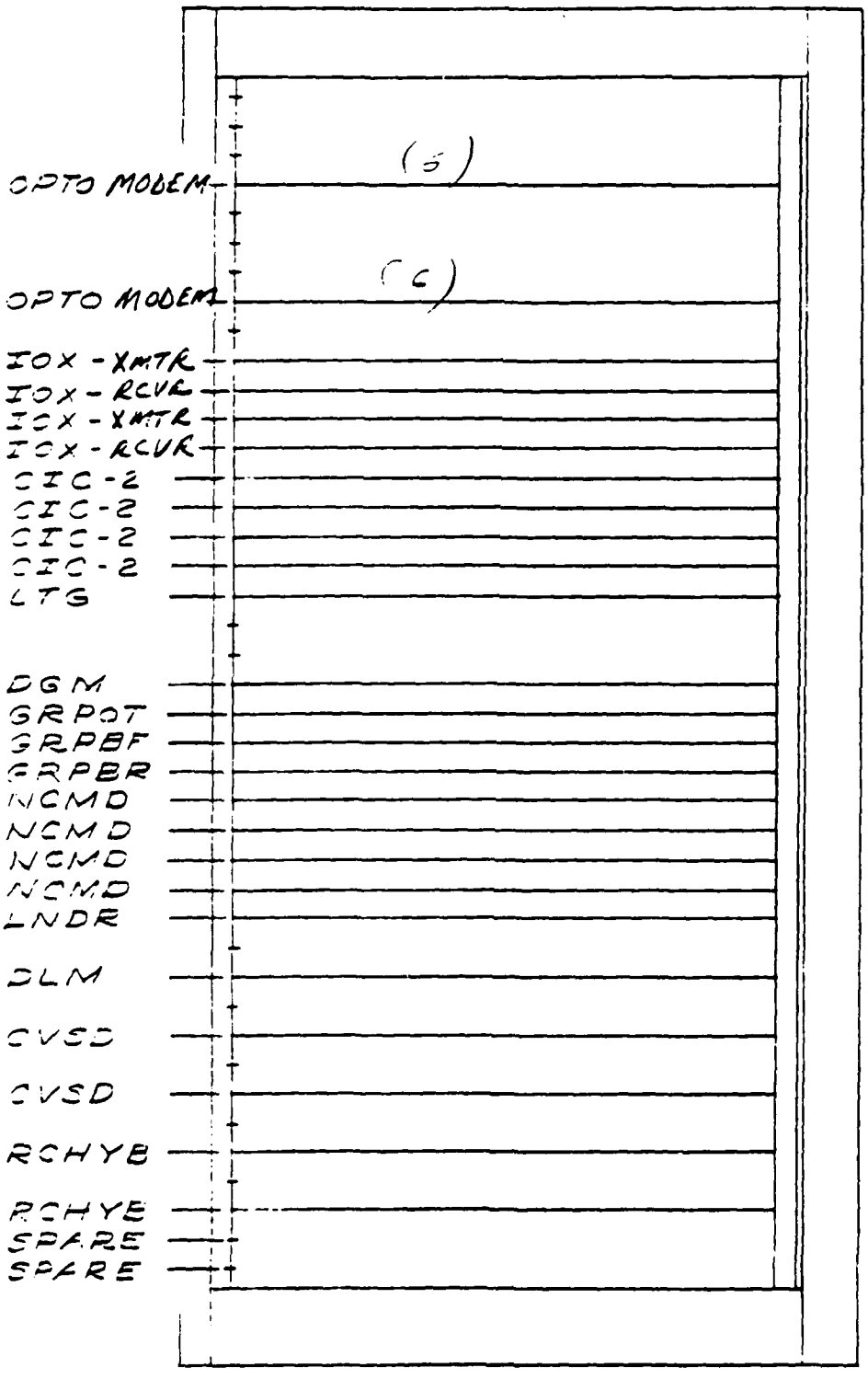


Figure 3-42 CIS Card Arrangment

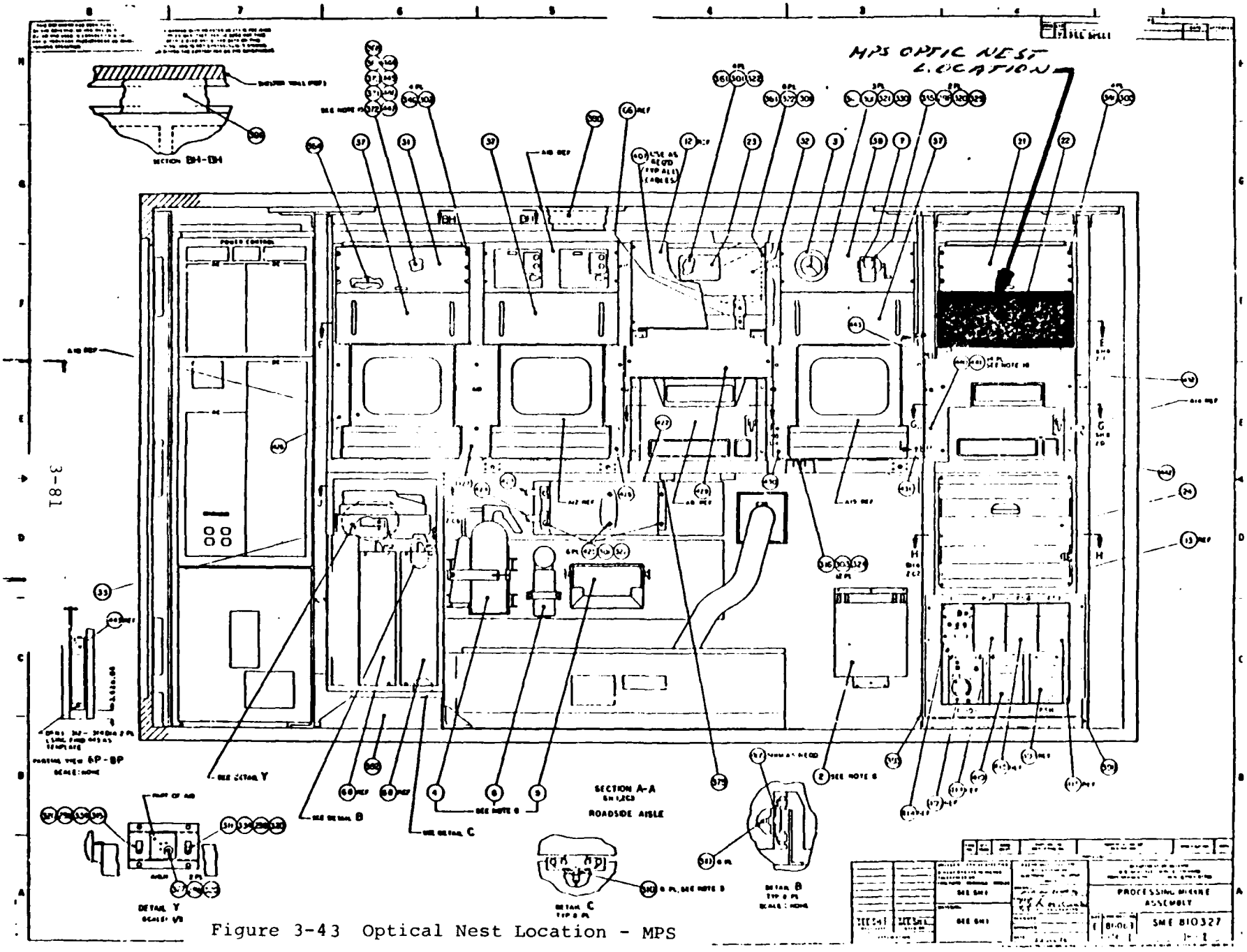


Figure 3-43 Optical Nest Location - MPS

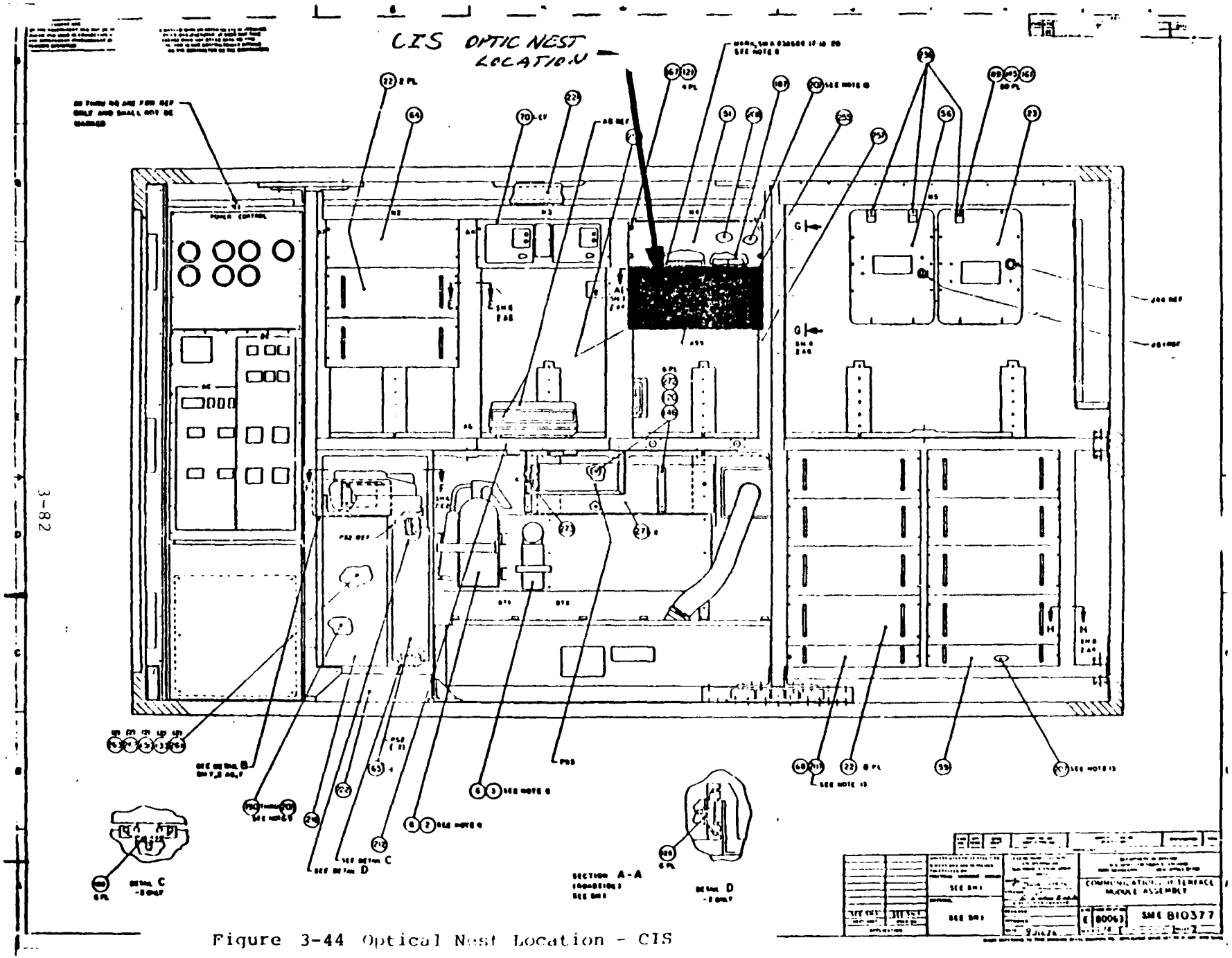


Figure 3-44 Optical Nest Location - CIS

PWB materials are in accordance with the Criteria Specification. Electrical cards shall use the AN/TTC-39 SM-A-838027-1 NAFI style connector. One hundred and twelve pins are provided on each connector. Optic cards shall interface with the nest backplane via a 24-pin card-mounted connector. This connector is described in Section 3.3.4.2.

3.3.4.1 TTC-39 Standard or Modified Cards

The following list includes all PWB assemblies which are standard AN/TTC-39 cards:

1. DLM-A, Digital Line MODEM-A, SM-E-809622
2. CVSD, Continuously Variable Slope Delta, SM-E-809563
3. NCMD, Nine Channel MUX/DEMUX, SM-E-809689
4. GRPFR, Group Framer, SM-E-809686
5. GRFBF, Group Buffer, SM-E-809687
6. GRPOT, Group Output, SM-E-810563
7. LTG, Local Timing Generator, SM-E-809625
8. CIC-2, I/O Transformer Interface, SM-E-809525

In addition, the CIC-2 (Var) and DGM Diphase Group Modem are similar to their respective standard AN/TTC-39 assemblies (SM-E-8-9525 and SM-E-809578) with the modification of deleted components.

3.3.4.2 New Cards

New PWB assemblies are as follows:

a. RCHYB, Resistor/Clock/Hybrid
b. LNDR, Line Driver/Receiver
c. IOX/XMTR
d. IOX/RCVR
e. Optical Modem

All new cards are designed in accordance with the AN/TTC-39 Criteria Specification SM-A-810507.

The connector used on the Optical Modem Card is a two-part assembly providing a 24-pin capability. The PWB design uses 18 pins comprised of six optical, six coaxial, and six power contacts , thereby leaving six available spares. As shown in Figure 3-45, the receptacle (PWB mounted) portion of the connector is riveted to the

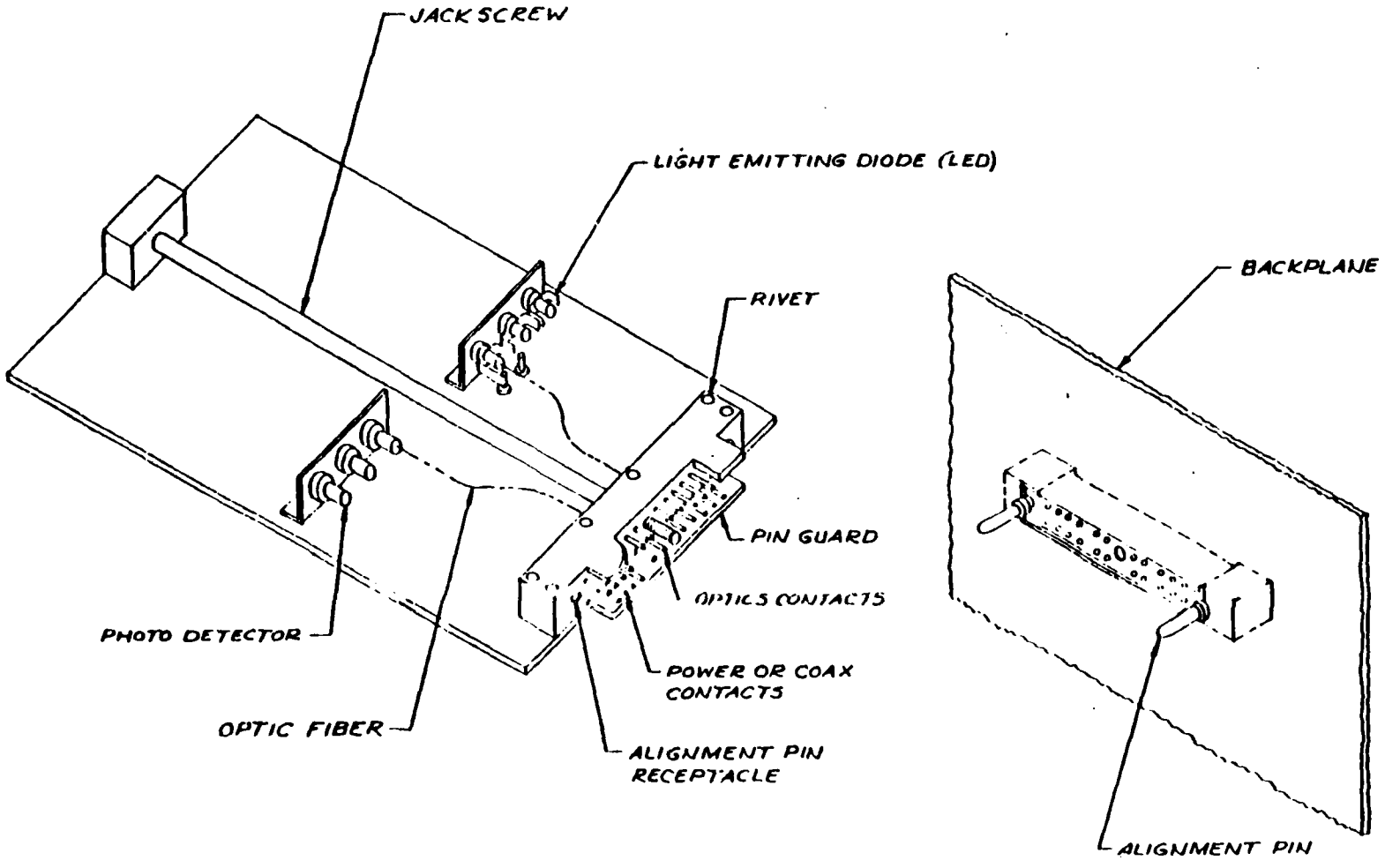


Figure 3-45 . Card Edge Connector Concept

board and uses two pins as locating devices rather than the rivets. The pin contacts are removable and are a size 16. The plug (backplane mounted) portion of the connector provides float both in and normal to the surface of the backplane and its socket contacts are also removable. Two locating dagger pins in the plug ensure alignment with the receptacle. A jack screw in the receptacle, which runs out to the opposite edge of the PWB, pulls together the two halves of the connector assembly. The jack screw is turned using a standard flat screwdriver in the slot at the free edge of the board, and the slot is recessed in a bracket to prevent slippage of the screwdriver. The optic contacts shown in Figure 3-45 float within the connector shells. A low-loss connection is ensured by an alignment bushing, which also provides a 0.001-inch gap by means of an integral spacer between the contacts. Photographs of the connectors are shown in Figures 3-46 and 3-47.

The optical cards also contain the light-emitting diodes (LED) and the photodetectors as described elsewhere. The photodetectors are mounted on a daughter-board which in turn is mounted directly to the PC card. The LEDs are mounted to standoffs. A photograph of the Optical Modem Card is shown in Figure 3-48.

3.3.5 Nest Power Requirements Summary

The power requirements for MPS and CIS optic nests are shown in Table 3-10. Voltages required are +5, -5, +12 and -12 volts. MPS and CIS maximum power is respectively 108 and 115 watts, and average power is 65 and 69 watts.

3.3.6 Internal Cable Assemblies

3.3.6.1 Configuration

The internal cables mate with the optical nest and with existing equipments within the shelter. The electrical signal cables are 26 twisted pair flat cables with connectors at each end. The cables in the CIC shelter are similar to those shown in Figure 3-49 and the cables in the MP shelter are similar to those shown in Figure 3-50.

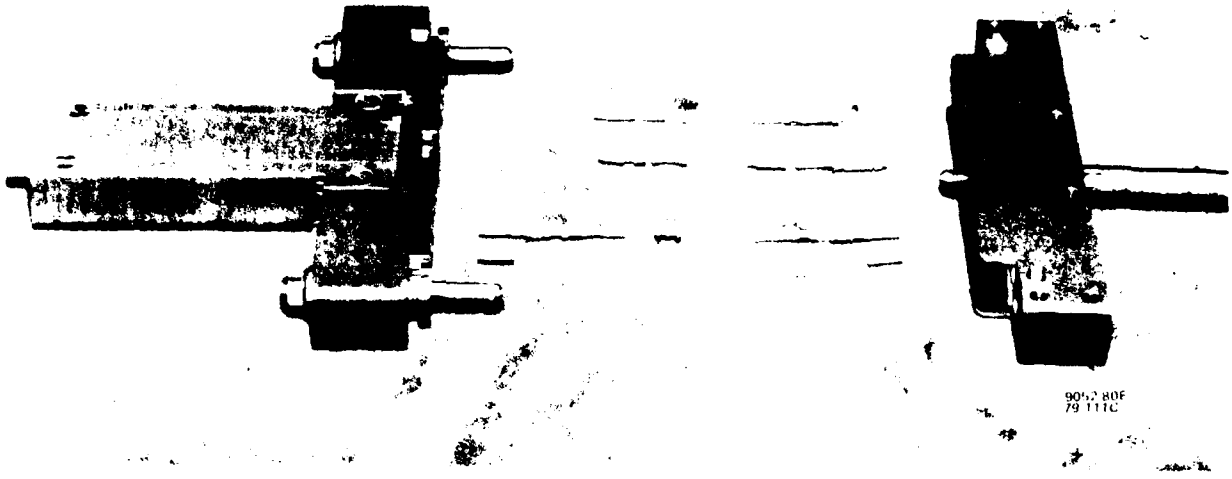


Figure 3-46. Multifunction (Optical/Electrical) Connector

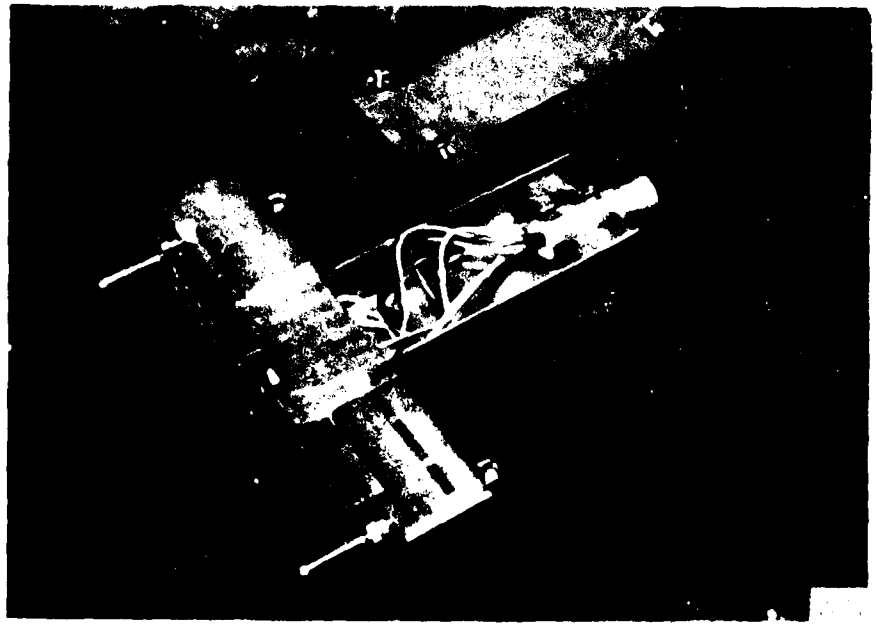


Figure 3-47. Optical Modem Card Connector - Nest Side

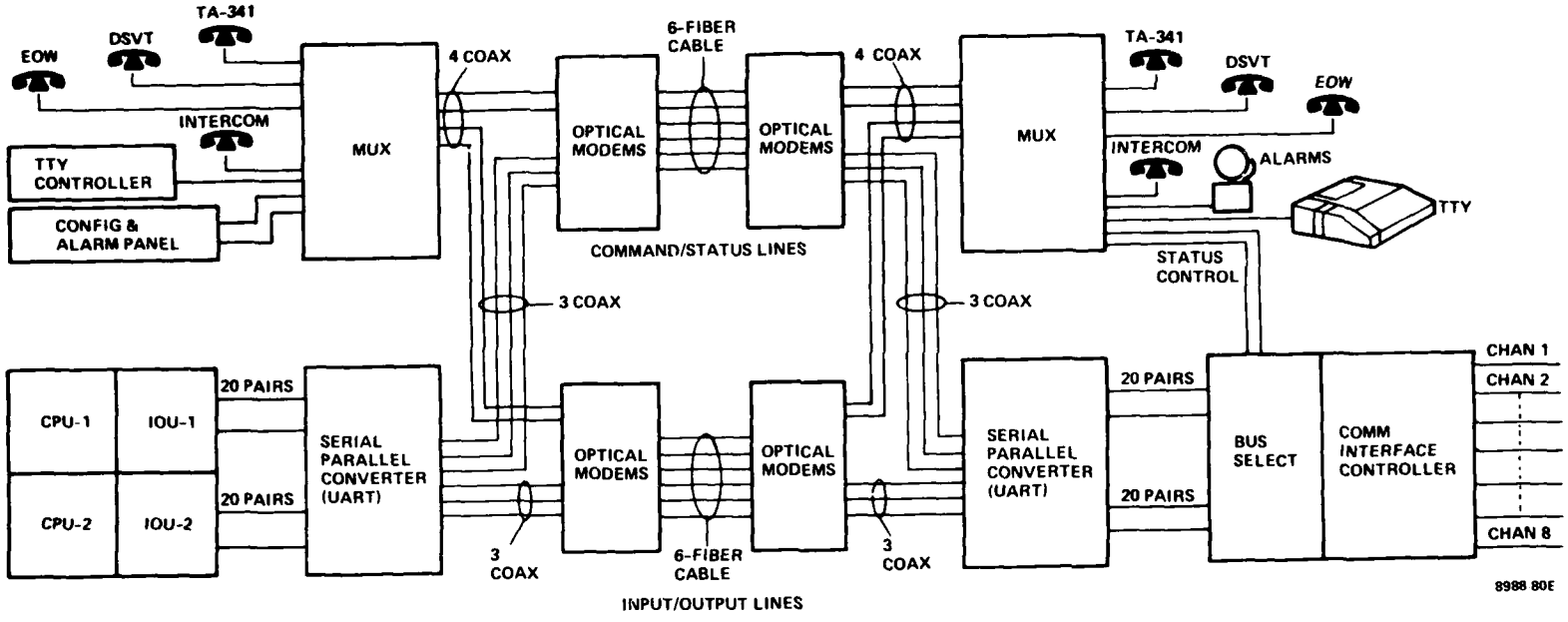


Figure 3-48 . Fully Assembled Optical Modem Card

TABLE 3-10. POWER SUPPLY SUMMARY

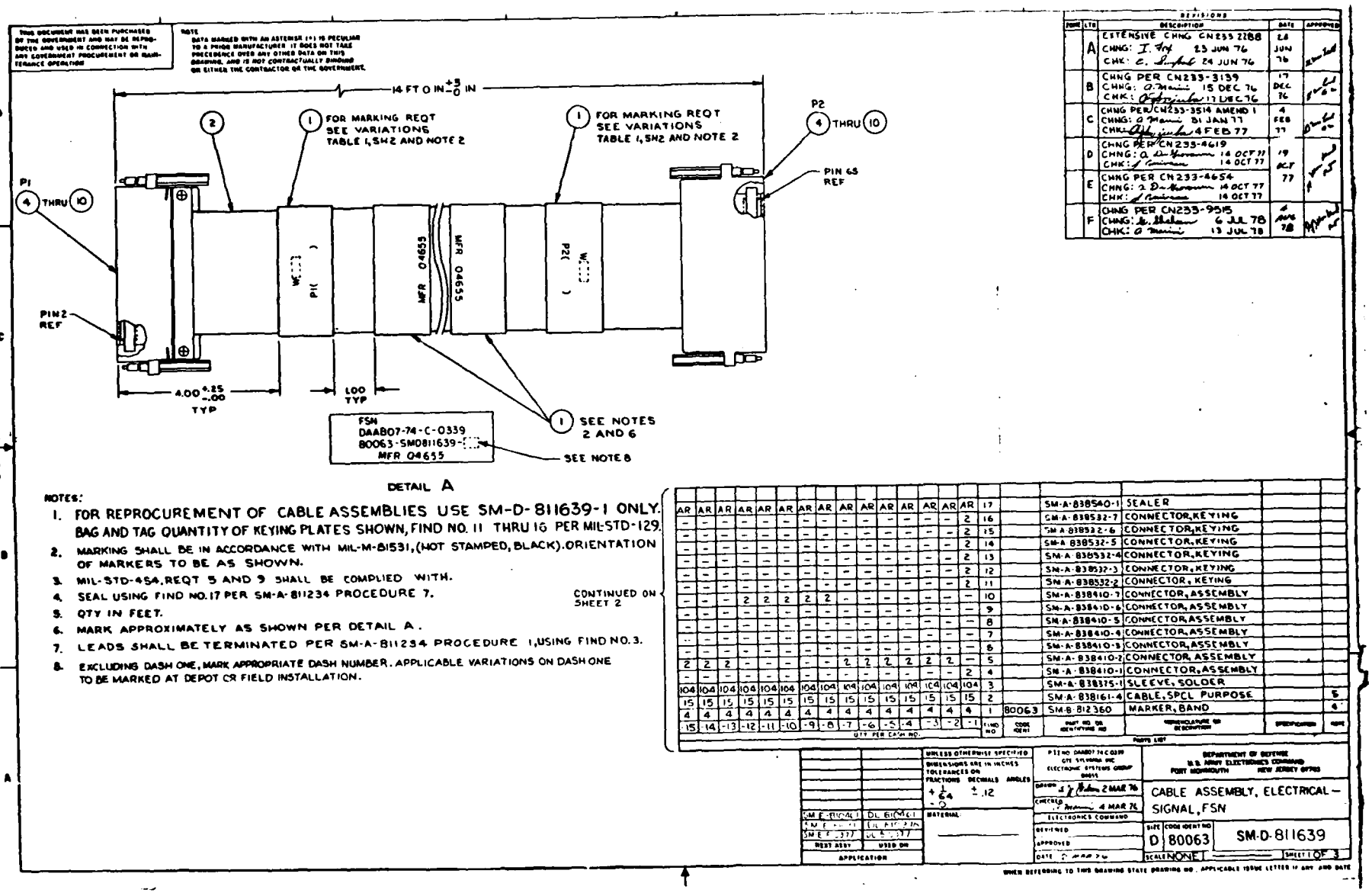
Card Type	+5V ma.	(+12) +15V	(-12) -15V	-5V	+5V Watts	+15V	-15V	-5V	Per Card Power Watts	MPS QTY	CIS QTY	MPS PWR Watts	PWR
DLM-A	350	50	10	40	1.75	0.75	0.15	0.20	2.85W	1	1	2.85	.2.85
CVSD	120	30	30	6	0.60	0.45	0.45	0.03	1.53	2	2	3.06	3.06
ICND	600	-	-	-	3.00	-	-	-	3.00	4	4	12.00	12.00
CRPFR CRTBF- CRPOT	2000	-	200	100	10.00	-	3.00	0.50	13.50	1	1	13.50	13.50
DGM	1200	6	0.2	80	6.00	0.09	0.01	0.40	6.50	1	1	6.50	6.50
RCHYB	92	+12 440	-12 440	-	0.46	5.28	5.28	-	11.02	2		22.04	22.04
LNDR	390			270	1.95			1.35	3.30	1	1	3.30	3.30
LTG	2410	-	-	30	12.05	-	-	0.150	12.20	1	1	12.20	12.20
IOX-1,2	1944	-	-	-	9.72	-	-	-	9.72	2	-	19.44	-
IOX-3,4	2640	-	-	-	13.20	-	-	-	13.20	-	2	-	26.40
CIC-2	613	-	-	65	3.07	-	-	0.33	3.40	2	-	6.80	-
CIC-2(VAR)	307	-	-	33	1.54	-	-	0.17	1.71	-	4	-	6.80
OPTO X/R	234	+12 118	-12 45	-	1.17	1.42	0.54	-	3.13	2	2	6.26	6.26
Totals												107.95	114.91

MPS	14756	1232	1240	662 ma
CIS	16150	1232	1240	662 ma

max values

+5 +12 -12 -5

108 Watts MPS Nest (65 Watt Average)
115 Watts CIS Nest (69 Watt Average)



DETAIL A

NOTES:

1. FOR REPROCUREMENT OF CABLE ASSEMBLIES USE SM-D-811639-1 ONLY. BAG AND TAG QUANTITY OF KEYING PLATES SHOWN, FIND NO. 11 THRU 16 PER MIL-STD-129.
2. MARKING SHALL BE IN ACCORDANCE WITH MIL-M-81531, (HOT STAMPED, BLACK). ORIENTATION OF MARKERS TO BE AS SHOWN.
3. MIL-STD-454, REQT 5 AND 9 SHALL BE COMPLIED WITH.
4. SEAL USING FIND NO. 17 PER SM-A-811234 PROCEDURE 7.
5. QTY IN FEET.
6. MARK APPROXIMATELY AS SHOWN PER DETAIL A.
7. LEADS SHALL BE TERMINATED PER SM-A-811234 PROCEDURE 1, USING FIND NO. 3.
8. EXCLUDING DASH ONE, MARK APPROPRIATE DASH NUMBER. APPLICABLE VARIATIONS ON DASH ONE TO BE MARKED AT DEPOT OR FIELD INSTALLATION.

CONTINUED ON SHEET 2

FIND NO.	QTY PER CAGE NO.	CAGE IDENT	PART NO. OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	NOTE
17	AR		SM-A-838540-1	SEALER		
16	2		SM-A-838532-7	CONNECTOR, KEYING		
15	2		SM-A-838532-6	CONNECTOR, KEYING		
14	2		SM-A-838532-5	CONNECTOR, KEYING		
13	2		SM-A-838532-4	CONNECTOR, KEYING		
12	2		SM-A-838532-3	CONNECTOR, KEYING		
11	2		SM-A-838532-2	CONNECTOR, KEYING		
10	-		SM-A-838410-7	CONNECTOR, ASSEMBLY		
9	-		SM-A-838410-6	CONNECTOR, ASSEMBLY		
8	-		SM-A-838410-5	CONNECTOR, ASSEMBLY		
7	-		SM-A-838410-4	CONNECTOR, ASSEMBLY		
6	-		SM-A-838410-3	CONNECTOR, ASSEMBLY		
5	2		SM-A-838410-2	CONNECTOR, ASSEMBLY		
4	-		SM-A-838410-1	CONNECTOR, ASSEMBLY		
3	104		SM-A-838375-1	SLEEVE, SOLDER		
2	15		SM-A-838161-4	CABLE, SPCL PURPOSE		5
1	4	80063	SM-B-812360	MARKER, BAND		6

PARTS LIST

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ESTENSIVE CHNG CN233 2188 CHNG: I. [illegible] 23 JUN 76 CHK: C. [illegible] 24 JUN 76	28 JUN 76	
	B	CHNG PER CN233-3139 CHNG: O. Marini 15 DEC 76 CHK: [illegible] 17 DEC 76	17 DEC 76	
	C	CHNG PER CN233-3514 AMEND 1 CHNG: O Marini 31 JAN 77 CHK: [illegible] 4 FEB 77	4 FEB 77	
	D	CHNG PER CN233-4619 CHNG: O. DeMarco 14 OCT 77 CHK: [illegible] 14 OCT 77	19 OCT 77	
	E	CHNG PER CN233-4654 CHNG: O. DeMarco 14 OCT 77 CHK: [illegible] 14 OCT 77	77	
	F	CHNG PER CN233-9515 CHNG: [illegible] 6 JUL 78 CHK: O Marini 13 JUL 78	6 JUL 78	

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ON FRACTIONS ±1/64, DECIMALS ±.12, ANGLES +0 -0
MATERIAL

PIT NO DAAB07-74-C-0339
CDT SYLVANIA GTE ELECTRONIC SYSTEMS GROUP 04655

DRAWN [illegible] 2 MAR 76
CHECKED [illegible] 4 MAR 76
ELECTRONICS COMMAND
DEVIATION
APPROVED
DATE [illegible]

DEPARTMENT OF DEFENSE
U.S. ARMY ELECTRONICS COMMAND
FORT MONMOUTH NEW JERSEY 07703

CABLE ASSEMBLY, ELECTRICAL — SIGNAL, FSN

SIZE D | CODE IDENT NO 80063 | SM-D-811639

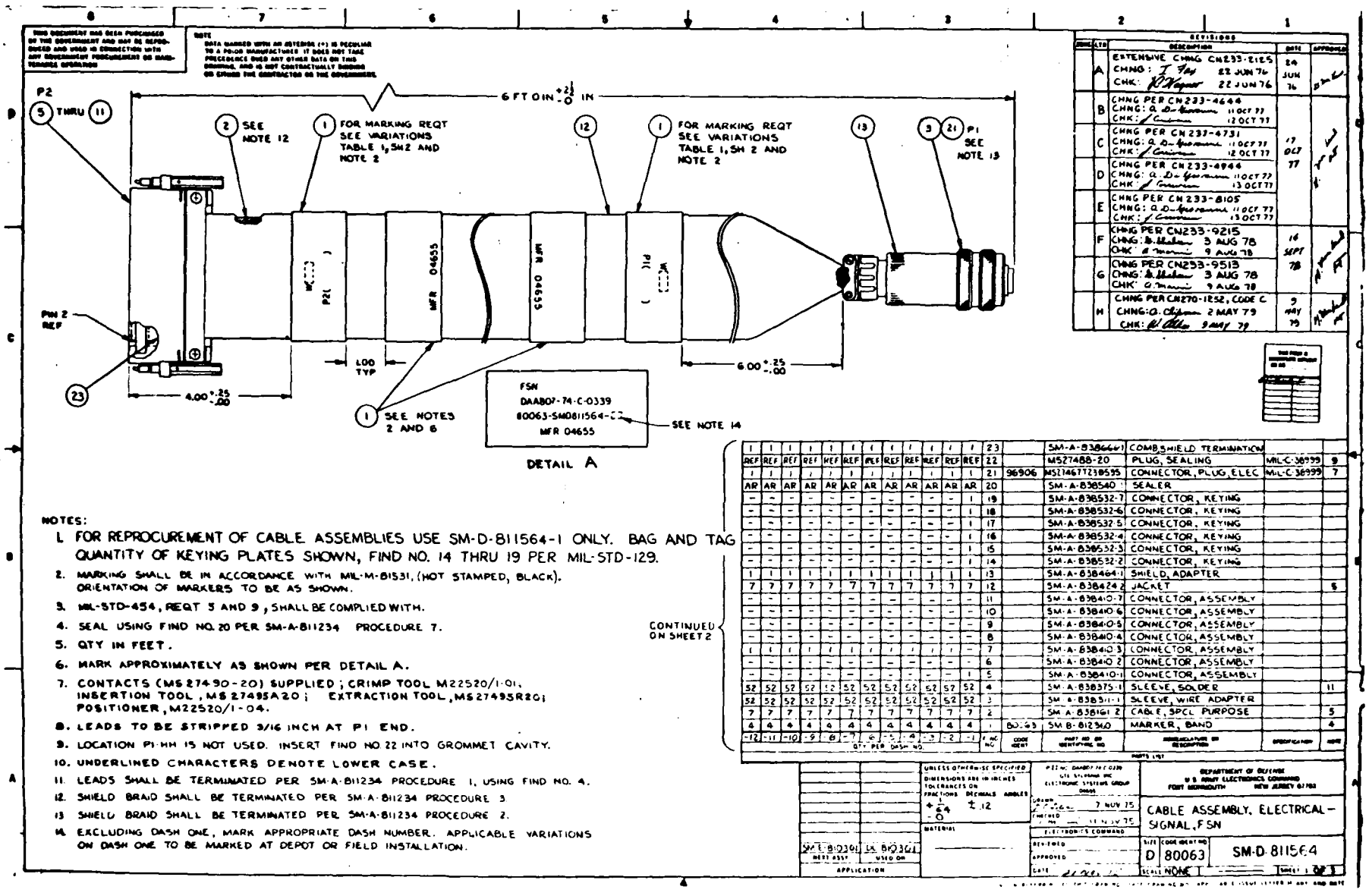
SCALE NONE | SHEET 1 OF 3

SM-E-811611 | DL 811611
SM-E-[illegible] | DL [illegible]
SHEET 3 OF 7 | DL [illegible]
NEXT ASSY | USED ON
APPLICATION

WHEN REFERRING TO THIS DRAWING STATE DRAWING NO., APPLICABLE ISSUE LETTER IF ANY AND DATE

3-89

Figure 3-49 - Cables - CI Shleter



ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	EXTENSIVE CHNG CN233-2125 CHNG: J. Fay 22 JUN 76 CHK: K.D. Wagner 22 JUN 76	24 JUN 76	
	B	CHNG PER CN233-4644 CHNG: Q. D. Yamamura 11 OCT 77 CHK: J. Cuevas 12 OCT 77		
	C	CHNG PER CN 233-4731 CHNG: Q. D. Yamamura 11 OCT 77 CHK: J. Cuevas 12 OCT 77	17 OCT 77	
	D	CHNG PER CN 233-4944 CHNG: Q. D. Yamamura 11 OCT 77 CHK: J. Cuevas 13 OCT 77		
	E	CHNG PER CN 233-8105 CHNG: Q. D. Yamamura 11 OCT 77 CHK: J. Cuevas 13 OCT 77		
	F	CHNG PER CN233-9215 CHNG: B. Hudson 3 AUG 78 CHK: A. Tamura 9 AUG 78	16 SEPT 78	
	G	CHNG PER CN233-9513 CHNG: B. Hudson 3 AUG 78 CHK: A. Tamura 9 AUG 78		
	H	CHNG PER CN270-1252, CODE C CHNG: G. Chipman 2 MAY 79 CHK: W. Allen 9 MAY 79	9 MAY 79	

NOTES:

1. FOR REPROCUREMENT OF CABLE ASSEMBLIES USE SM-D-811564-1 ONLY. BAG AND TAG QUANTITY OF KEYING PLATES SHOWN, FIND NO. 14 THRU 19 PER MIL-STD-129.
2. MARKING SHALL BE IN ACCORDANCE WITH MIL-M-81531, (HOT STAMPED, BLACK). ORIENTATION OF MARKERS TO BE AS SHOWN.
3. MIL-STD-454, REQT 5 AND 9, SHALL BE COMPLIED WITH.
4. SEAL USING FIND NO. 20 PER SM-A-811234 PROCEDURE 7.
5. QTY IN FEET.
6. MARK APPROXIMATELY AS SHOWN PER DETAIL A.
7. CONTACTS (MS 27490-20) SUPPLIED; CRIMP TOOL M22520/1-01, INSERTION TOOL, MS 27495A20; EXTRACTION TOOL, MS 27495R20; POSITIONER, M22520/1-04.
8. LEADS TO BE STRIPPED 3/16 INCH AT P1 END.
9. LOCATION P1-HH IS NOT USED. INSERT FIND NO 22 INTO GROMMET CAVITY.
10. UNDERLINED CHARACTERS DENOTE LOWER CASE.
11. LEADS SHALL BE TERMINATED PER SM-A-811234 PROCEDURE 1, USING FIND NO. 4.
12. SHIELD BRAID SHALL BE TERMINATED PER SM-A-811234 PROCEDURE 3
13. SHIELD BRAID SHALL BE TERMINATED PER SM-A-811234 PROCEDURE 2.
14. EXCLUDING DASH ONE, MARK APPROPRIATE DASH NUMBER. APPLICABLE VARIATIONS ON DASH ONE TO BE MARKED AT DEPOT OR FIELD INSTALLATION.

CONTINUED ON SHEET 2

QTY PER DASH NO. -12	-11	-10	-9	-8	-7	-6	-5	-4	-3	-2	-1	FIND NO.	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION	SPECIFICATION	NOTE
1	1	1	1	1	1	1	1	1	1	1	1	23		SM-A-838666-1	COMB, SHIELD TERMINATION		
REF	REF	REF	REF	REF	REF	REF	REF	REF	REF	REF	REF	22		M527488-20	PLUG, SEALING	MIL-C-38999	9
1	1	1	1	1	1	1	1	1	1	1	1	21	96906	MS21467T23B35S	CONNECTOR, PLUG, ELEC	MIL-C-38999	7
AR	AR	AR	AR	AR	AR	AR	AR	AR	AR	AR	AR	20		SM-A-838540-1	SEALER		
-	-	-	-	-	-	-	-	-	-	-	1	19		SM-A-838532-7	CONNECTOR, KEYING		
-	-	-	-	-	-	-	-	-	-	-	1	18		SM-A-838532-6	CONNECTOR, KEYING		
-	-	-	-	-	-	-	-	-	-	-	1	17		SM-A-838532-5	CONNECTOR, KEYING		
-	-	-	-	-	-	-	-	-	-	-	1	16		SM-A-838532-4	CONNECTOR, KEYING		
-	-	-	-	-	-	-	-	-	-	-	1	15		SM-A-838532-3	CONNECTOR, KEYING		
-	-	-	-	-	-	-	-	-	-	-	1	14		SM-A-838532-2	CONNECTOR, KEYING		
1	1	1	1	1	1	1	1	1	1	1	1	13		SM-A-838464-1	SHIELD, ADAPTER		
7	7	7	7	7	7	7	7	7	7	7	7	12		SM-A-838424-2	JACKET		5
-	-	-	-	-	-	-	-	-	-	-	-	11		SM-A-838410-7	CONNECTOR, ASSEMBLY		
-	-	-	-	-	-	-	-	-	-	-	-	10		SM-A-838410-6	CONNECTOR, ASSEMBLY		
-	-	-	-	-	-	-	-	-	-	-	-	9		SM-A-838410-5	CONNECTOR, ASSEMBLY		
-	-	-	-	-	-	-	-	-	-	-	-	8		SM-A-838410-4	CONNECTOR, ASSEMBLY		
1	1	1	1	1	1	1	1	1	1	1	1	7		SM-A-838410-3	CONNECTOR, ASSEMBLY		
-	-	-	-	-	-	-	-	-	-	-	-	6		SM-A-838410-2	CONNECTOR, ASSEMBLY		
-	-	-	-	-	-	-	-	-	-	-	1	5		SM-A-838410-1	CONNECTOR, ASSEMBLY		
52	52	52	52	52	52	52	52	52	52	52	52	4		SM-A-838375-1	SLEEVE, SOLDER		11
52	52	52	52	52	52	52	52	52	52	52	52	3		SM-A-838511-1	SLEEVE, WIRE ADAPTER		
7	7	7	7	7	7	7	7	7	7	7	7	2		SM-A-838161-2	CABLE, SPCL PURPOSE		5
4	4	4	4	4	4	4	4	4	4	4	4	1	80063	SM-B-812340	MARKER, BAND		4

PARTS LIST

NEXT ASSY	USED ON
SM-E-810391	LA 810361

APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS +1/64 -0, DECIMALS ±.12, ANGLES

MATERIAL

PREPARED UNDER THE DIRECTION OF U.S. SIGNAL INC ELECTRONIC SYSTEMS GROUP DAYTON

DRAWN 7 NOV 75
TRACED 11 NOV 75
ELECTRONICS COMMAND

REVIEWED
APPROVED
DATE 21 NOV 75

DEPARTMENT OF DEFENSE
U.S. ARMY ELECTRONICS COMMAND
FORT MONMOUTH NEW JERSEY 07703

CABLE ASSEMBLY, ELECTRICAL - SIGNAL, FSN

SIZE D | CODE IDENT NO 80063 | SM-D-811564

SCALE NONE | SHEET 1 OF 3

3-90

Figure 3-50 Cables - MP Shelter

In the MP shelter, one end of each cable has a 66-pin NAFI style blade-and-fork connector that will mate with the input/output connector of the nest. The other end of the cable has a bulkhead style connector that mates with the connector that normally goes to the SEP. This particular style cable is a jumper cable which goes from the optical nest to the equipment intended utilizing the existing cabling.

In the CI shelter, the cables have NAFI-style connectors on each end of the cables. These cables will replace existing cables, and are used to connect the optical nest with the intended equipments (see Figure 3-52).

The connector at each end of the cables have keying plates to prevent improper connection. The wires are soldered to the connector contacts. Latching pins are provided on the connector to ensure that the connectors will remain mated, even under transport conditions.

In the MP shelter, power cables are drawn from the VDU/CAP nest. Extra flexible hook-up wires as presently being used in the AN/TYC-39 are brought from the rear power distribution bracket of the nest, along the inside wall of the shelter to the rear of the LDFOCCS nest. Number four wire is used for the +5 VDC and number 10 is used for all other voltages.

In the CI shelter, power is brought out on the CIC nest. Wires are routed along the inside curbside wall, across the front inside wall of the shelter, then to the LDFOCCS nest along the inside roadside wall of the shelter. The sizes are as in the MP shelter.

3.3.6.2 Routing

Routing of the cables from the optics nest to the intended equipments is as shown in Figures 3-51 and 3-52. Cabling is emplaced within existing cable troughs.

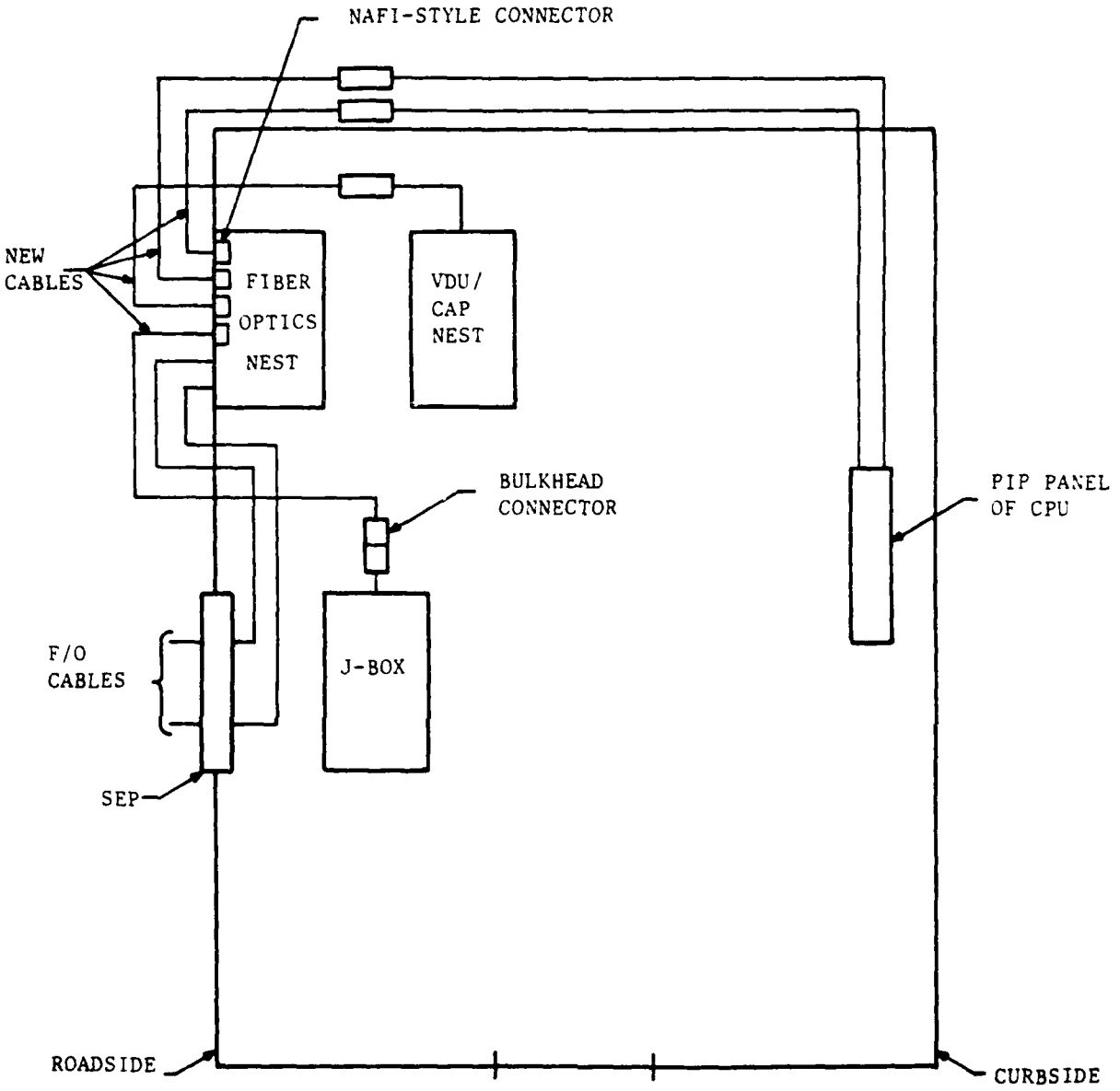


Figure 3-51 New MSMP Cabling

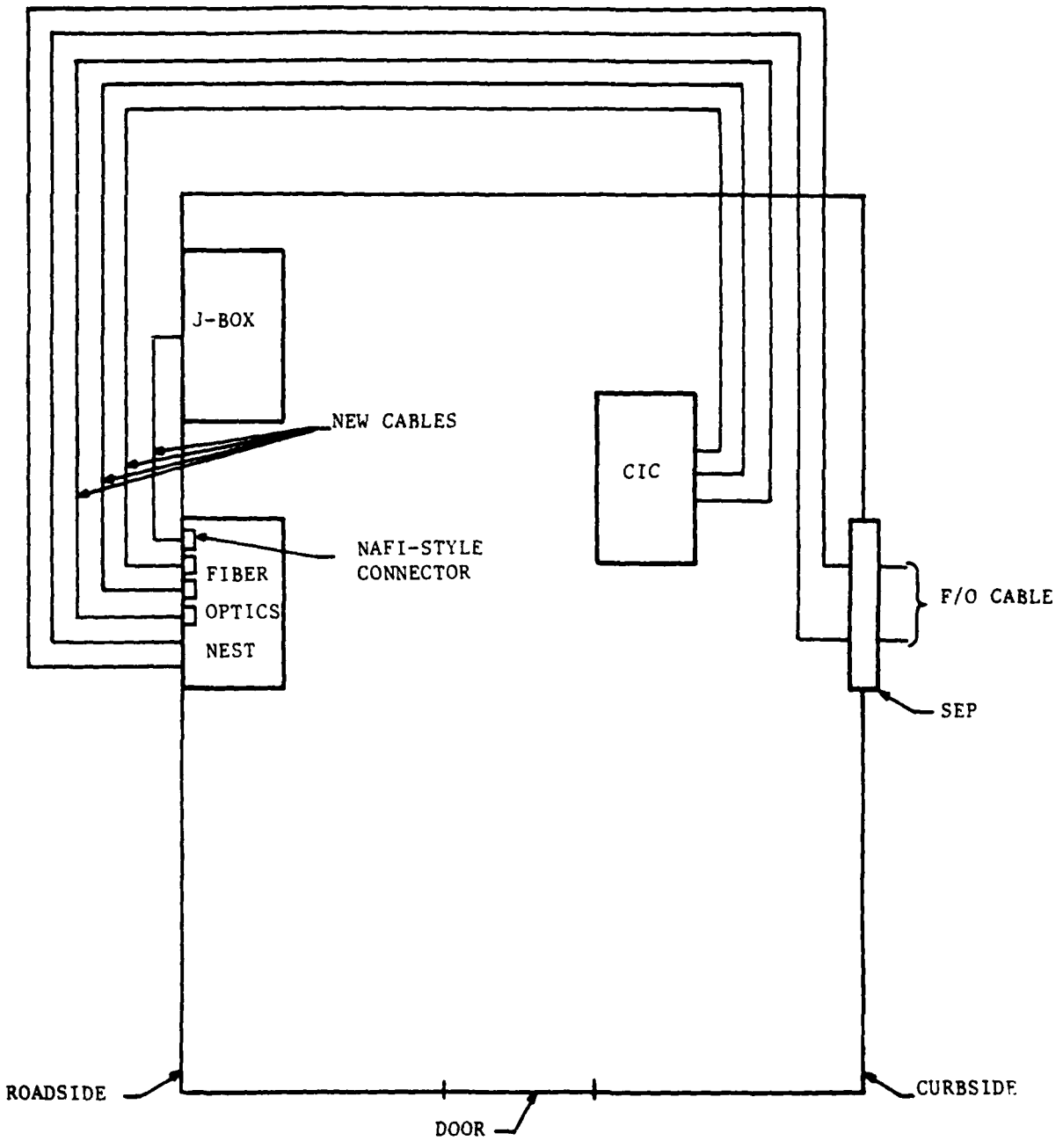


Figure 3- 52 New CIS Cabling

In the MP shelter, as shown in Figure 3-51, one cable is routed from the nest to the junction box, one from the nest to the VDU/CAP nest, and two cables from the nest to the PIP panel of the CPU. Normally, each of these units have their cables terminate at the signal entry panel (SEP); however, with the optics nest in place, they mate with the cable jumpers from the nest.

The two optical cables are routed from the SEP directly the optical connector located on the rear of the nest. The nest is located on the same side (roadside) as the SEP; hence, optical cable lengths have been minimized.

In the CI shelter, as shown in Figure 3-52, three cables are routed from the optics nest to the CIC and one cable from the nest to the J. Box. New cables are provided for the shelter. The optical cabling comes from curbside to roadside is routed across the front wall of the shelter behind the existing sheet metal cable protectors; hence, they are not visible from inside the shelter.

3.3.7 SEP Modifications

Both the MPS SEP (SM-D-835644) and CIS SEP (SM-D-835652) presently provide for the mounting of four input/output electrical signal connectors: i.e., J6, J8, J9, and J10.

In the MPS SEP, plates are bolted to the holes occupied by J10 and J9 to provide EMI, RFI and weather-tight integrity to the shelter. The J7 and J8 holes are filled with the optical cable connector receptacles.

The CIS cable configuration (see Section 3.3.6.1) allows both the J9 and J10 connectors to remain in place on the SEP. As above, the optical cable connector receptacles fill J7 and J8.

APPENDIX A

OPERATIONAL TEST PROCEDURE

APPLICATION	
NEXT ASSY	USED ON
	LDOFCCS

REVISIONS			
LTR	DESCRIPTION	DATE	APPROVED

REV																													
SHEET	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60
REV	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—						
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30

REVISION RECORD STATUS OF SHEETS

UNLESS NOTED DIM. ARE IN INCHES. TOLERANCES .XX ± ANGLES .XXX ± ±	CONTRACT NO. DAAK80-79-0508	GTE SYLVANIA INC ELECTRONIC SYSTEMS GROUP – EASTERN DIVISION NEEDHAM HEIGHTS, MASSACHUSETTS
	DWN J Hamilton DATE 3 Jan 1980	
	CHK	OPERATIONAL TEST PROCEDURE
MATERIAL	APVD	
	APVD	
	RELEASE APVD	SIZE A / CODE IDENT NO. 04655 / DRAWING NO. 00-1363487
		SCALE / REV — / SHEET 1 OF 24

FORM ESG-ED 1224.3 (4-74)

TABLE OF CONTENTS

	SIZE	CODE IDENT NO.	DRAWING NO.	
	A	04655	00-1363487	
	SCALE		REV —	SHEET 2

FORM ESG-ED 1224.4 (4-74)

LIST OF ILLUSTRATIONS

	SIZE	CODE IDENT NO.	DRAWING NO.	
	A	04655	00-1363487	
	SCALE		REV —	SHEET 3

LIST OF TABLES

	SIZE	CODE IDENT NO.	DRAWING NO.
	A	04655	00-1363487
	SCALE		REV — SHEET 4

FORM ESG-ED 1224.4 (4-74)

LIST OF TESTS

	SIZE	CODE IDENT NO.	DRAWING NO.	
	A	04655	00-1363487	
	SCALE		REV —	SHEET 5

FORM ESG-ED 1224.4 (4-74)

LIST OF TEST EQUIPMENT

Unit Under Test Chassis Assembly (P/N 01-1363975)

IOX Tester Assembly (P/N 01-1363974)

Oscilloscope, Tektronix Model 454 or equivalent

Audio Oscillator, Hewlett Packard Model 200CD or equivalent

Loop Back Module Assembly (P/N 01-1363973)

	SIZE	CODE IDENT NO.	DRAWING NO.	
	A	04655	00-1363487	
	SCALE		REV —	SHEET 6

FORM ESG-ED 1224.4 (4-74)

LIST OF TERMS AND ABBREVIATIONS

BER	Bit Error Rate
CIS	Communications Interface Shelter
MPS	Message Processing Shelter
UUT	Unit Under Test
BP	Binding Post

SIZE	CODE IDENT NO.	DRAWING NO.
A	04655	00-1363487
SCALE		REV — SHEET 7

FORM ESG-ED 1224.4 (4-74)

TEST PROCEDURES

	SIZE	CODE IDENT NO.	DRAWING NO.	
	A	04655	00-1363487	
	SCALE		REV —	SHEET 8

FORM ESG-ED 1224.4 (4-74)

FUNCTIONAL PERFORMANCE TEST

	SIZE	CODE IDENT NO.	DRAWING NO.
	A	04655	00-1363487
	SCALE		REV — SHEET 9

FORM ESG-ED 1224.4 (4-74)

ITEM	ACTION	OBSERVATION	✓
1	Power up system and set controls as shown in Table 1.	Lights illuminate randomly.	
2	Press the Request/Indicator Reset Switch.	Request and Indicator lights extinguish.	
3	Press the Bit Error Counter Reset Switch.	Bit error lights extinguish, MPS to CIS light bank and CIS to MPS light bank display stable random patterns.	
4	Set the MPS to CIS switch bank as indicated in Line 1 of Table 2. Press the Request/Indicator Reset Switch, then press the Bit Error Counter Reset Switch.	MPS to CIS light bank matches the setting of the MPS to CIS switch bank and is stable. Note that the light bank is read from bottom to top while the switch bank is read from top to bottom. CIS to MPS light bank displays a stable random pattern. Request and Indicator lights are extinguished. Bit Error lights are extinguished.	
5	Wait 5 seconds.	MPS to CIS light bank remains stable. Bit Error lights remain extinguished.	
6	Repeat steps 4 and 5 for lines 2 through 5 of Table 2.	MPS to CIS light bank matches switch bank and no bit errors are detected for five seconds.	
7	Set all switches in the MPS to CIS bank to Ø. Set the rotary function switch to "CIS to MPS".	Lights illuminate randomly.	
8	Set the CIS to MPS switch bank as indicated in Line 6 of Table 2. Press the Request/Indicator Reset Switch, then press the Bit Error Counter Reset Switch.	CIS to MPS light bank matches the setting of the CIS to MPS switch bank and is stable. MPS to CIS light bank displays a stable random pattern. Request and Indicator lights are extinguished. Bit Error Lights are extinguished.	
9	Wait 5 seconds	CIS to MPS light bank remains stable. Bit Error lights remain extinguished.	
10	Repeat steps 8 and 9 for lines 7 through 9 of Table 2.	CIS to MPS light bank matches switch bank and no bit errors are detected for five seconds. The indicator light is extinguished	

SIZE	CODE IDENT NO.	DRAWING NO.
A	04655	00-1363487
SCALE		REV — SHEET 10

FORM ESG-ED 1224.4 (4-74)

ITEM	ACTION	OBSERVATION	✓
		for line 7 and illuminates for lines 8 and 9. The request lights remain extinguished.	
11	Set the CIS to MPS switch bank as indicated in line 10 of Table 2. Press the Request/Indicator Reset Switch.	Request lights Ø through 3 illuminate, lights 4 through 7 remain extinguished. Other lights illuminate randomly.	
12	Repeat step 11 for line 11 of Table 2.	Request lights 4 through 7 illuminate, lights Ø through 3 are extinguished.	
13	Repeat Step 11 for Line 12 of Table 2.	Request lights Ø, 2, 4, 6 illuminate, lights 1, 3, 5, 7 are extinguished.	
14	Repeat Step 11 for Line 13 of Table 2.	Request lights 1, 3, 5, 7 illuminate, lights Ø, 2, 4, 6 are extinguished.	
15	Repeat Step 11 for Line 14 of Table 2.	All request lights illuminate.	
16	Set the CIS to MPS switch bank as indicated in Line 15 of Table 2. Press the Request/Indicator Reset Switch.	Request lights 1 and 6 illuminate, lights 0, 2, 3, 4, 5, and 7 are extinguished. Other lights illuminate randomly.	
17	Set the rotary function switch to "ALTERNATE". Set the switch banks as indicated in Line 16 of Table 2. Press the Request/Indicator Reset Switch, then press the Bit Error Counter Reset Switch.	MPS to CIS light bank matches the MPS to CIS switch bank. CIS to MPS light bank displays a stable random pattern. Indicator light illuminates. Request lights are extinguished.	
18	Repeat Step 17 for Lines 17 through 20 of Table 2.	CIS to MPS light bank matches the CIS to MPS switch bank. Other lights are as specified in Step 17.	
19	Set the rotary function switch to "MANUAL".	None.	
20	Connect an oscilloscope to BP1 (signal) and BP4 (ground).	The oscilloscope displays a 16.384 MHz square wave of at least 0.4 volts peak to peak.	

SIZE	CODE IDENT NO.	DRAWING NO.
A	04655	00-1363487
SCALE		REV — SHEET 11

FORM DSG-ED 1224.4 (4-74)

ITEM	ACTION	OBSERVATION	✓
21	Move the oscilloscope signal input lead from BP1 to BP2.	Same as in step 20.	
22	Move the oscilloscope signal input lead from BP2 to BP6. Connect an audio oscillator to BP6 (signal) and BP7 (ground). Set the oscillator for a 1 kHz, 1 volt peak to peak sine wave. Move the oscilloscope input lead from BP6 to BP8. Set the Amplifier Enable Switch to "ENABLE".	The oscilloscope displays a 1 kHz sine wave of between 8 volts peak to peak and 10 volts peak to peak.	
23	Set the Amplifier Enable Switch to "DISABLE".	The oscilloscope indicates no signal present.	
24	Connect BP8 to BP3. Move the oscilloscope input lead from BP8 to BP5.	The oscilloscope indicates a DC level of zero volts.	
25	Set the Amplifier Enable switch to "ENABLE".	The oscilloscope indicates a DC level of +5 volts.	
26	Disconnect the audio oscillator and oscilloscope.	None	
27	Set switches S1 and S2 as indicated in the first line of Table 3. Press the CLOCK pushbutton (as indicated by the "X" in the CLOCK column of Table 3).	Lights L1 and L2 match the first line of Table 3(Ø = OFF, 1 = ON).	
28	Repeat Step 27 for each remaining line in Table 3. The entries must be performed in the order given, and if a mistake is made in activating the switches the test must be restarted at the beginning.	Lights L1 and L2 match the corresponding entries in Table 3.	
29	Repeat Steps 27 and 28 using Table 4. Set switches S1 and S2 as indicated, and press the CLOCK or CLEAR button if an "X" is present in the appropriate column for that entry.	For each step lights L3 through L6 match the corresponding entries in Table 4.	
30	Shut off power to the system.	All lights extinguish.	

SIZE	CODE IDENT NO.	DRAWING NO.
A	04655	00-1363487
SCALE		REV — SHEET 12

FORM ESG-ED 1224.4 (4-74)

BIT ERROR RATE TEST

	SIZE	CODE IDENT NO.	DRAWING NO.	
	A	04655	00-1363487	
	SCALE		REV —	SHEET 13

FORM ESG-ED 1224.4 (4-74)

ITEM	ACTION	OBSERVATION	✓
1.	Disconnect the UUT Chassis from the 10X Tester by unplugging the power and signal cables at the UUT end. Connect the Loop Back Module to the Tester as follows:	None.	
1.a	Connect plugs J1 and J2 of the signal cables into their correspondingly numbered sockets on the Loop Back Module.	None.	
1.b	Connect the power wire pins from the Loop Back Module into the correspondingly lettered sockets of the power cable connector.	None.	

SIZE	CODE IDENT NO.	DRAWING NO.
A	04655	00-1363487
SCALE		REV --- SHEET 13A

FORM ESG-D 1224.4 (4-74)

ITEM	ACTION	OBSERVATION	✓
2.	Power up the system and set the controls as shown in Table 5.	Lights illuminate randomly.	
3.	Press the Request/Indicator Reset Switch, then press the Bit Error Counter Reset Switch.	Request lights, indicator light, and Bit Error lights extinguish. MPS to CIS light bank matches the MPS to CIS switch bank. CIS to MPS light bank matches the CIS to MPS switch bank.	
4.	Let the tester run for 4 hours.	At the end of the 4 hour period, record the number of Bit Errors, as counted by the Bit Error lights. Bit Errors:_____	
5.	Shut off power to the system.	All lights extinguish.	
6.	Disconnect and remove the Loop Back Module. Reconnect the power and signal cables to the UUT chassis.	None.	
7.	Power up the system and set the controls as shown in Table 5.	Lights illuminate randomly.	
8.	Press the Request/Indicator Reset Switch, then press the Bit Error Counter Reset Switch.	Request lights, indicator light, and Bit Error lights extinguish. MPS to CIS light bank matches the MPS to CIS switch bank. CIS to MPS light bank matches the CIS to MPS switch bank.	
9.	Let the tester run for 4 hours.	At the end of the 4 hour period, record the number of Bit Errors as counted by the Bit Error lights. Bit Errors:_____	

SIZE	CODE IDENT NO.	DRAWING NO.
A	04655	00-1363487
SCALE		REV SHEET 14

ITEM	ACTION	OBSERVATION	✓
10.	Subtract the number of Bit Errors recorded in Step 4 from the number of Bit Errors recorded in Step 9.	The result must be less than or equal to 3. If the result is greater than 3, continue for 4 hours. After 8 hours, the result must be equal to or less than 6 errors.	
11.	Shut off power to the system.	All lights extinguish.	

SIZE	CODE IDENT NO.	DRAWING NO.
A	04655	00-1363487
SCALE		REV

SHEET 15

FORM DD ED 1224.4 (4-74)

TABLES AND FIGURES

	SIZE	CODE IDENT NO.	DRAWING NO.
	A	04655	00-1363487
	SCALE		REV -- SHEET 16

FORM ESG-ED 1224.4 (4-74)

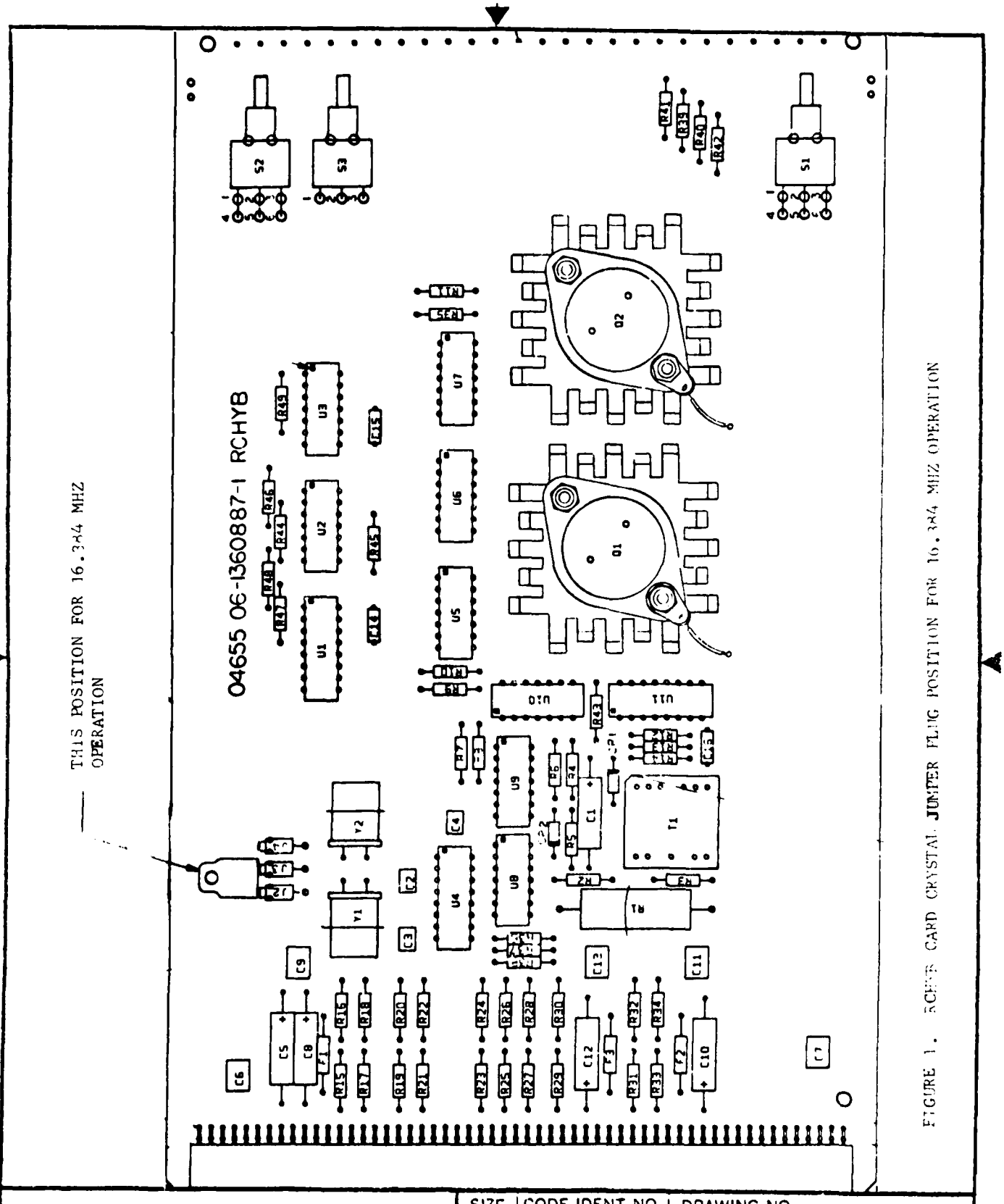


FIGURE 1. SCHEM CARD CRYSTAL JUMPER PLUG POSITION FOR 16.384 MHZ OPERATION

SIZE	CODE IDENT NO.	DRAWING NO.
A	04655	00-1363487
SCALE		REV — SHEET 17

FORM ESG-ED 1224.4 (4-74)

TABLE 1

Initial Control Settings

Tester Front Panel

MPS to CIS Switch Bank: All Switches to "Ø" (Down)

CIS to MPS Switch Bank: All Bit Switches to "Ø", All Request/Data Switches to "D".

Rotary Function Switch: "MPS to CIS".

Byte Rate Potentiometer: 600 nanoseconds

Burst Rate Potentiometer: 100 microseconds

UUT Chassis

Short/Long Switch: "NORMAL"

RCHYB Card Switches: Positions are unimportant

RCHYB Card Crystal Select Jumper Plug:
16.384 MHz position (See Figure 1)

	SIZE	CODE IDENT NO.	DRAWING NO.
	A	04655	00-1363487
	SCALE		REV — SHEET 18

FORM ESG-ED 1224.4 (4-74)

	MPS TO CIS						CIS TO MPS			
LINE	ROW 1	ROW 2	ROW 3	ROW 4	ROW 5	ROW 6	ROW 1	ROW 2	ROW 3	ROW 4
1	E0	E1	E2	E3	E4	E5				
2	E6	E7	E6	E6	E7	E7				
3	EC	C	C	1	2	3				
4	4	5	6	7	P	P				
5	C1357	0246P	C1357	0246P	C01234567P	C01234567P				
6							0	1	2	3
7							4	5	6	7
8							P	I	P	I
9							0246P	1357I	0246P	01234567PI
10							R0	R1	R2	R3
11							R4	R5	R6	R7
12							R0246			
13							R1357			
14							R01234567			
15							01234567P	R1	4	R6

TABLE 2. IOX TEST PATTERNS

FORM ESG-ED 1224.4 (4-74)

SIZE A | CODE IDENT NO. 04655 | DRAWING NO. 00-136387 | SCALE | REV — | SHEET 19

MPS To CIS							CIS TO MPS			
LINE	ROW 1	ROW 2	ROW 3	ROW 4	ROW 5	ROW 6	ROW 1	ROW 2	ROW 3	ROW 4
16	C	E2	C	E2	C	E2	I	I	I	I
17	E2	C	E2	C	E2	C	I	I	I	I
18	C	E2	C	E2	C	E0	0	0	0	0
19	C	E1	C	E1	C	E1	0	0	0	0
20	C1357	0246P	C1357	0246P	C1357	0246P	0246P	1357I	0246P	1357I

TABLE 2. (CONTINUED)

To interpret the data in this table:

The data patterns are listed by giving the non-zero bits in each byte. Thus, "2567" indicates that bits 2, 5, 6, and 7, are set to a logic "1" and all other bits are set to a logic "0". The bytes are read from the switch bank in top to bottom order. Also, "E" refers to the Enable bit, "C" refers to the Command bit, "I" refers to the Indicator bit, and (in the CIS to MPS link only) an "R" preceding a byte indicates that the Request/Data switch is set to the Request position (the Data position is used otherwise). A blank row indicates that all switches in that row are set to "0".

SET SWITCHES		PRESS BUTTONS			OBSERVE LIGHTS		
S1	S2	CLOCK	CLEAR		L1	L2	✓
0	0	X			0	0	
0	0	X			0	0	
0	1	X			0	1	
0	1	X			0	1	
1	1	X			0	1	
1	0	X			0	1	
0	0	X			0	0	
1	0	X			1	0	
1	0	X			1	0	
1	1	X			1	0	
0	1	X			1	0	
0	0	X			0	0	
1	1	X			0	1	
0	0	X			0	0	

TABLE 3. INTERCOM CONTROL LOGIC TEST PATTERNS

SIZE	CODE IDENT NO.	DRAWING NO.
A	04655	00-1363487
SCALE		REV — SHEET 21

FORM ESG-ED 1224.4 (4-74)

SET SWITCHES		PRESS BUTTONS			OBSERVE LIGHTS				
S1	S2	CLOCK	CLEAR		L3	L4	L5	L6	√
0	0		X		0	0	0	0	
0	0	X			0	0	0	0	
0	0	X			0	0	0	0	
0	0	X			0	0	0	0	
0	0	X			0	0	0	0	
1	0	X			1	1	0	0	
1	0	X			0	0	0	0	
1	0	X			0	1	1	0	
1	0	X			0	0	0	1	
0	0	X			0	0	0	1	
0	0	X			0	0	0	1	
0	0	X			0	0	0	1	
0	0	X			0	0	0	0	
1	0	X			1	1	0	0	
0	0	X			0	0	0	0	
1	0	X			1	1	1	0	
1	1				0	0	0	0	
0	1				0	0	0	0	

TABLE 4. TGM SYNC LOGIC TEST PATTERNS

SIZE	CODE IDENT NO.	DRAWING NO.
A	04655	00-1363487
SCALE		REV — SHEET 22

FORM ESG-ED 1224.4 (4 74)

SET SWITCHES		PRESS BUTTONS		OBSERVE LIGHTS				
S1	S2	CLOCK	CLEAR	L3	L4	L5	L6	✓
0	0			1	1	1	0	
0	0	X		0	0	0	1	
0	1			0	0	0	1	
0	0			0	0	0	1	
0	0	X		0	1	1	0	
0	0	X		0	0	0	1	
0	0	X		0	0	0	0	

TABLE 4. (CONTINUED)

SIZE	CODE IDENT NO.	DRAWING NO.
A	04655	00-1363487
SCALE		REV — SHEET 23

FORM ESG-ED 1224.4 (4-74)

APPENDIX B

IOX TESTER AND UUT CHASSIS DESCRIPTION

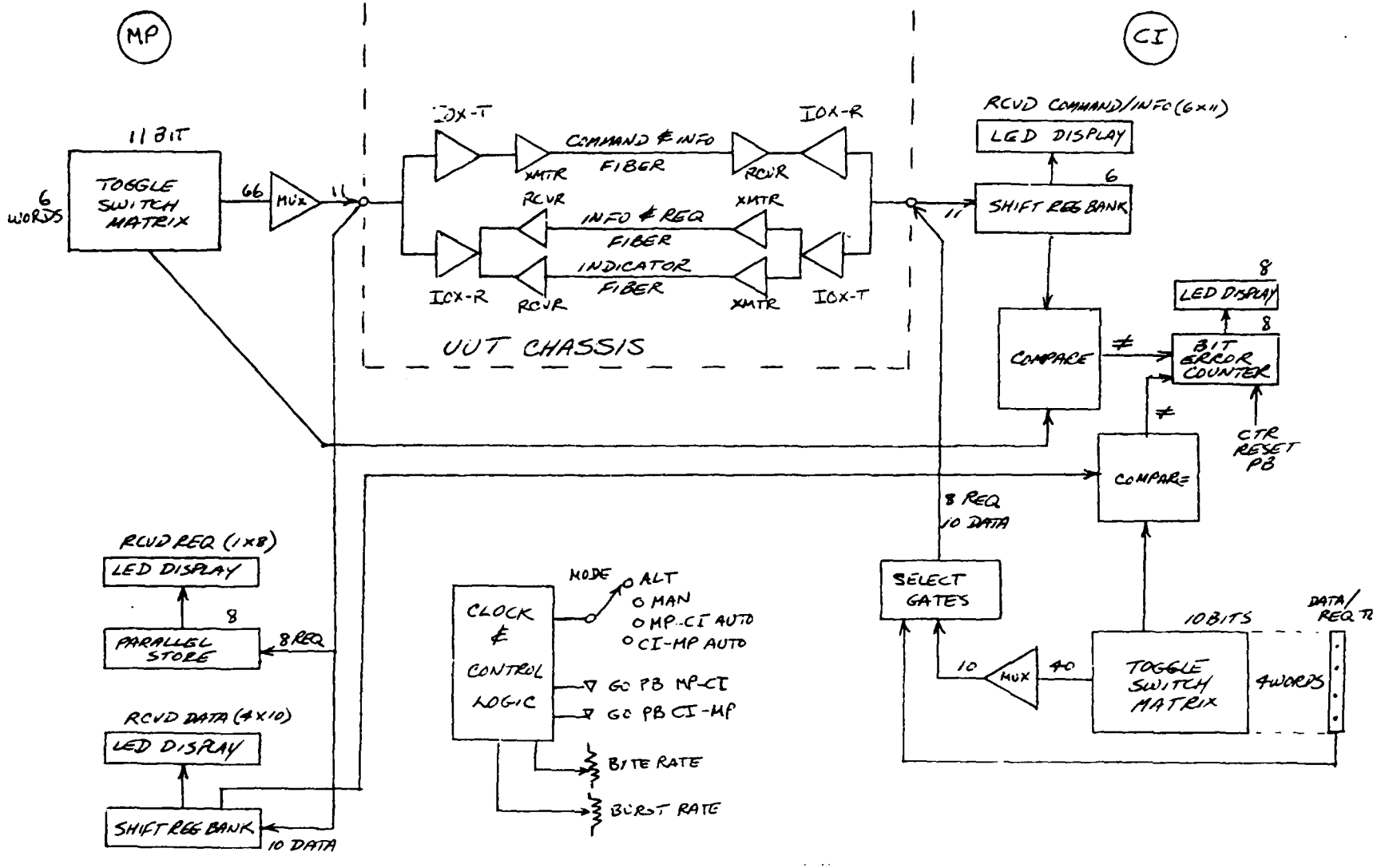


Figure B-1 IOX Link Tester Block Diagram

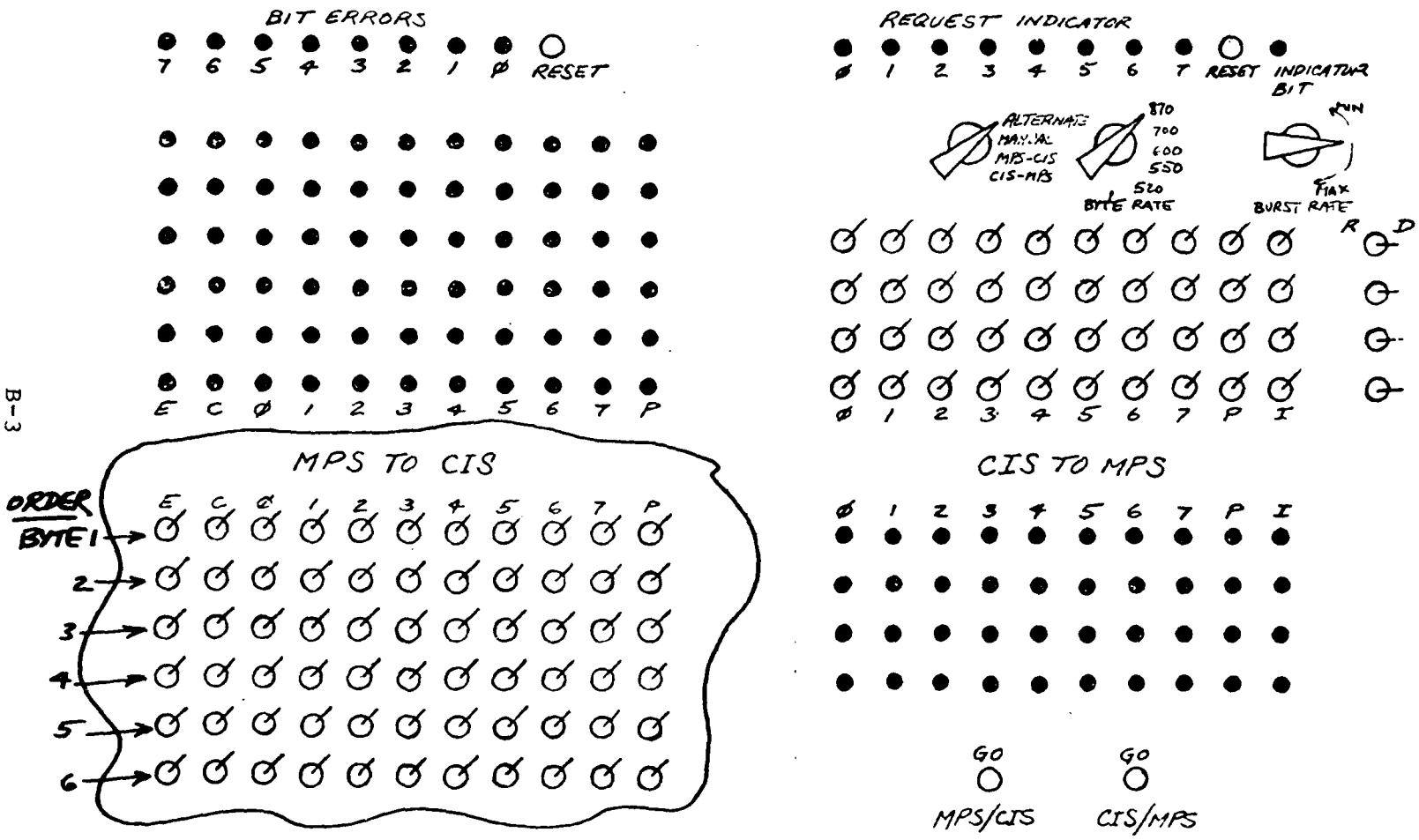


FIGURE B-2 - IOX LINK TESTER PANEL

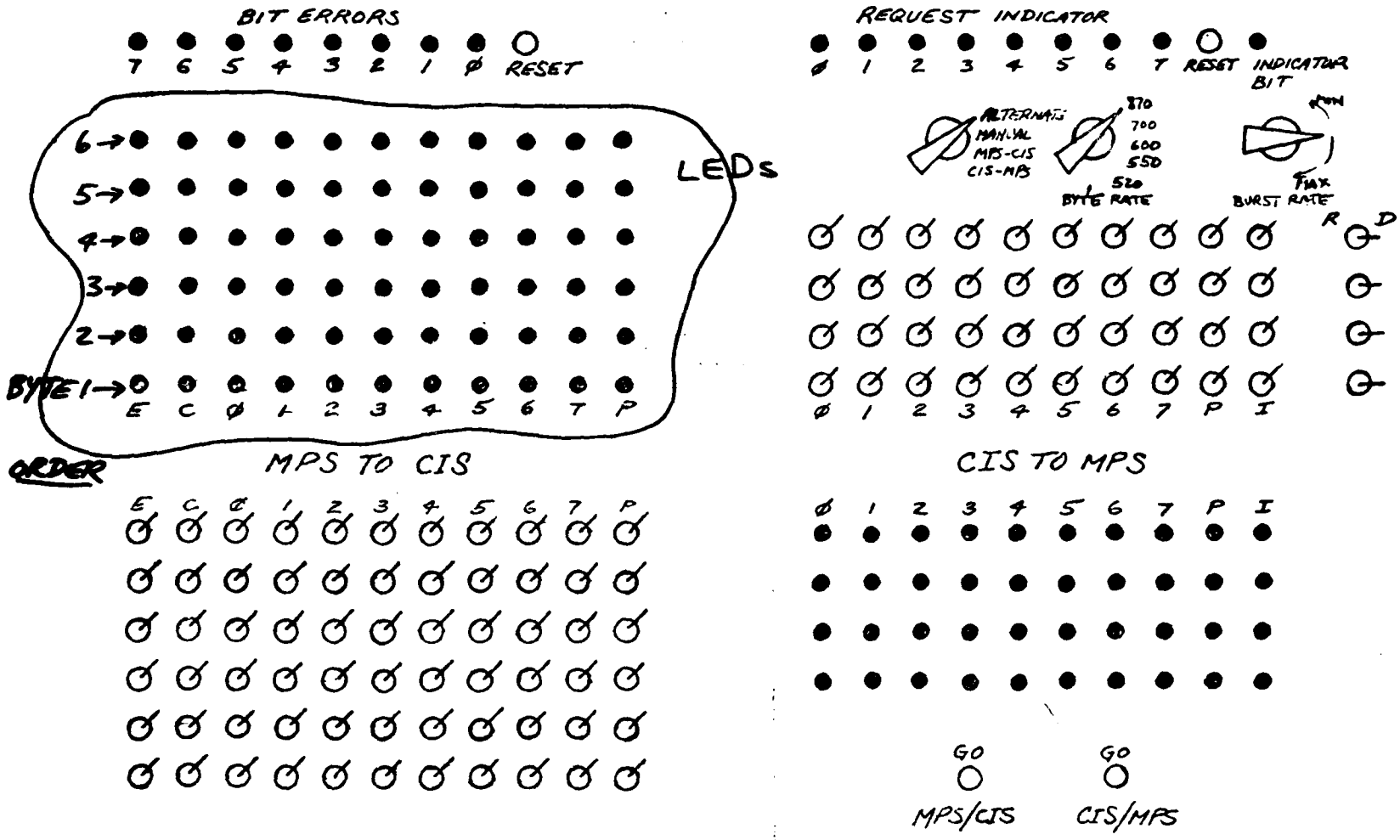


FIGURE B-3 - IOX LINK TESTER PANEL

The received bytes are compared against the original content of the switches for equality and errors are recorded in the BIT ERROR COUNTER as they are detected (fig. B-4). The counter will accumulate the error count until reset by its COUNTER RESET PB (fig. B-4). Transmission in the reverse direction is similar except that the 4X10 switch matrix is used to represent either the Information bits or Request bits in the transmission (fig. B-5). A toggle at the end of each row is used to designate whether the row contains data or requests (fig. B-5). At the receiving end of the link, data is stored in banks of serial shift while requests are stored in cummulative parallel storage, and are separately displayed on LEDs (fig. B-6). In this direction of communication, comparisons are also made against the original content of the toggle switches, and discrepancies are counted in the same BIT ERROR COUNTER (fig. B-4).

The tester has byte rate and burst rate oscillators with front panel control of each (fig. B-7). In the Manual Mode, the MP-CI and CI-MP GO bushbuttons will initiate an operation in the indicated direction (fig. B-8). One depression of the button will generate one burst of bytes from the designated toggle switch bank. The bytes will be spaced according to the BYTE RATE potentiometer (range = 520 to 800 NSEC). The CI-MP AUTO MODE will repeat similarly. The ALTERNATE MODE will alternately trigger bursts of data in the two directions the frequency of alternation being under control of the BURST RATE potentiometer (range = 3.6 usec to 144 usec). With these control options, delay analyses can be verified in the breadboard cards as well as in the qualification of the production card designs (better than in the actual system). Specific processor IOX

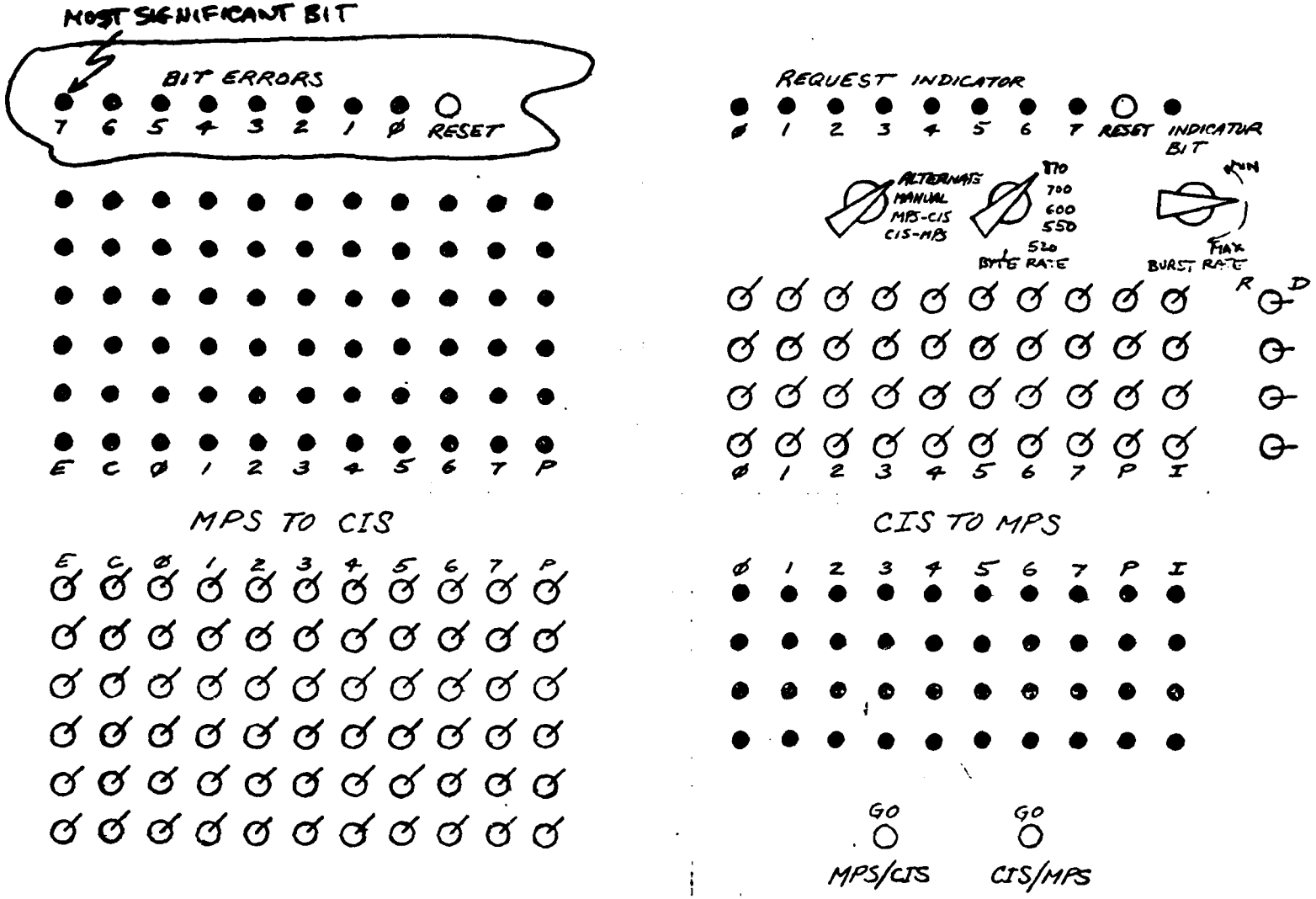


FIGURE B-4 -IOX LINK TESTER PANEL

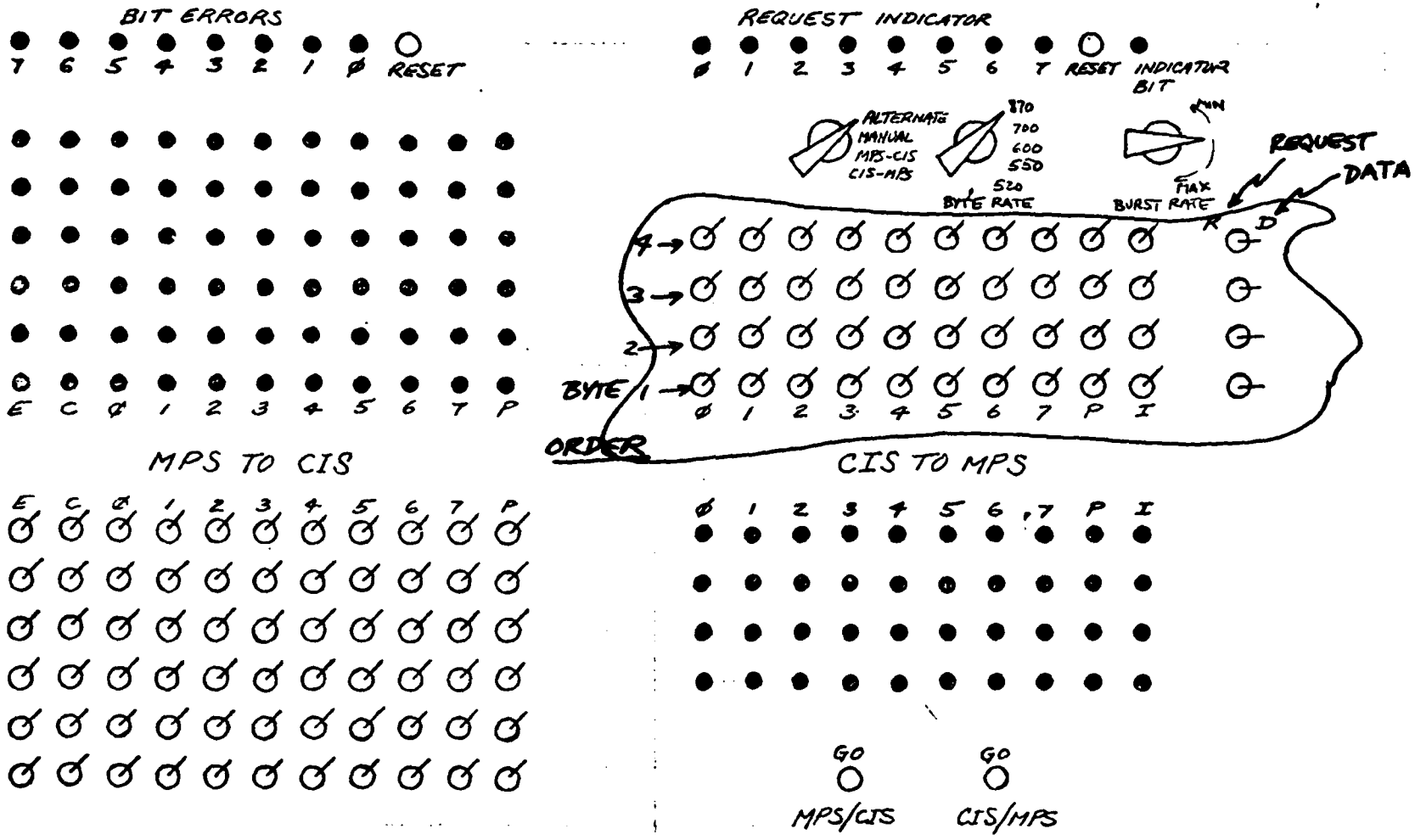


FIGURE B-5 -IOX LINK TESTER PANEL

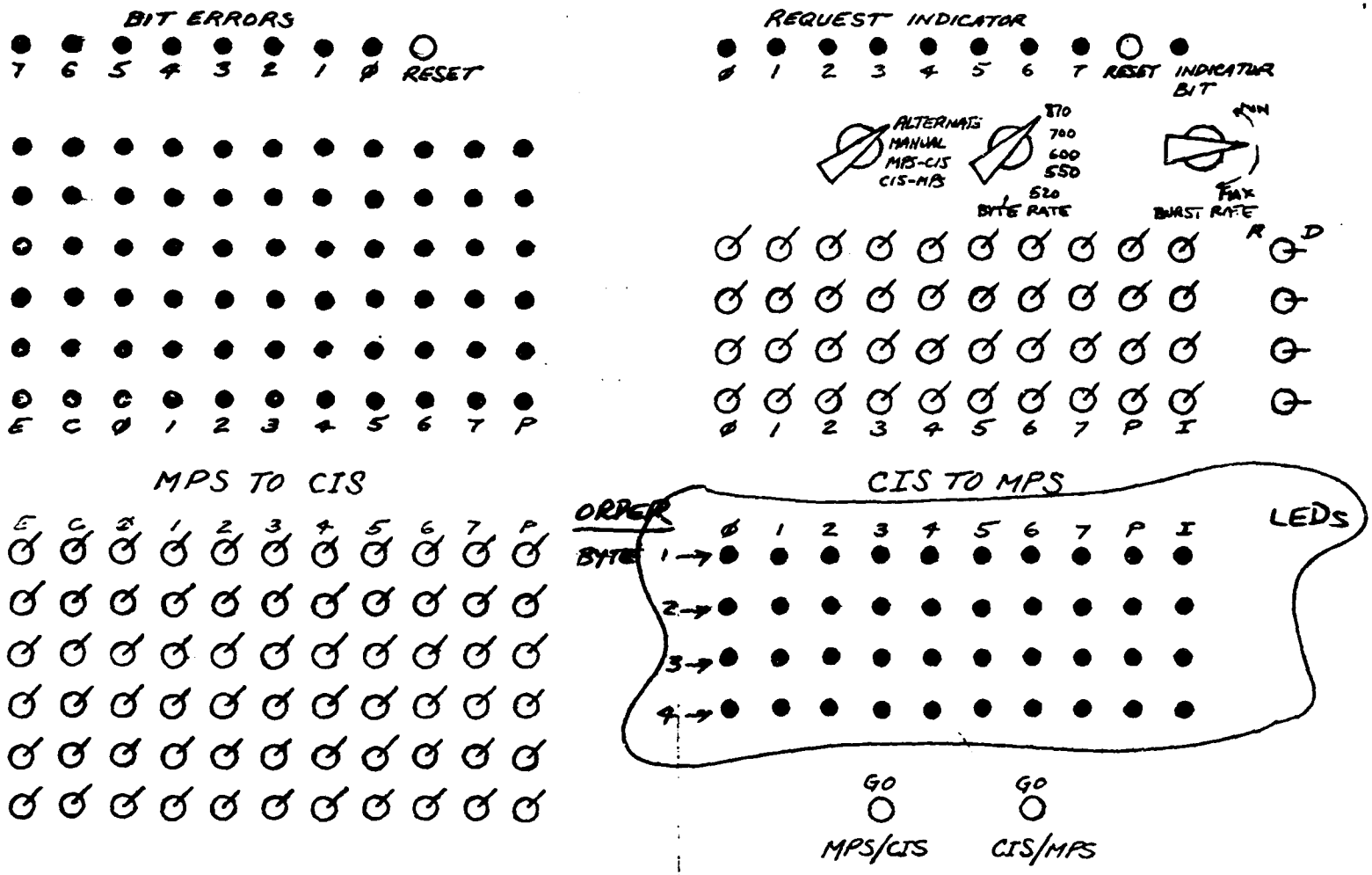


FIGURE B-6-IOX LINK TESTER PANEL

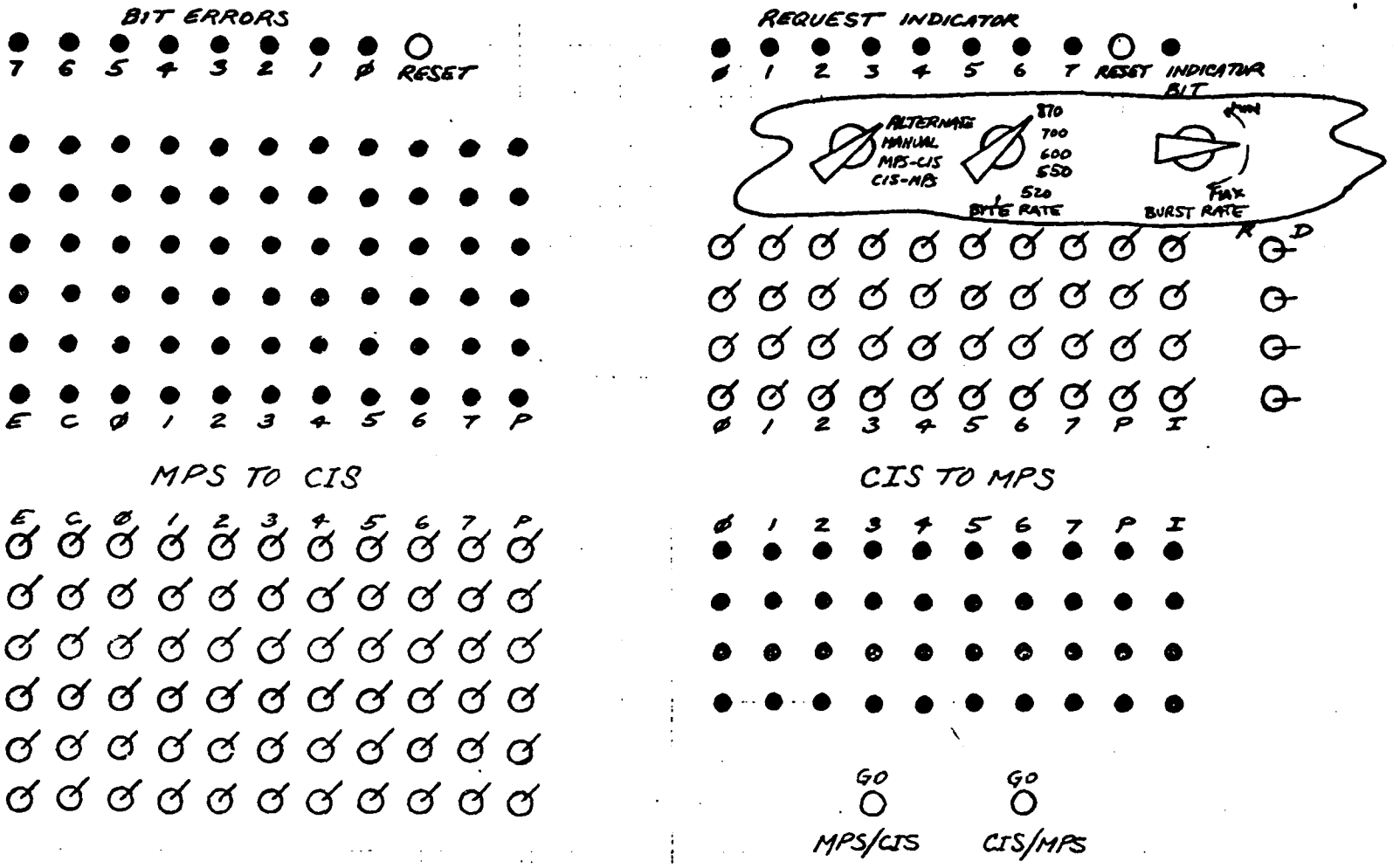


FIGURE B-7 - IOX LINK TESTER PANEL

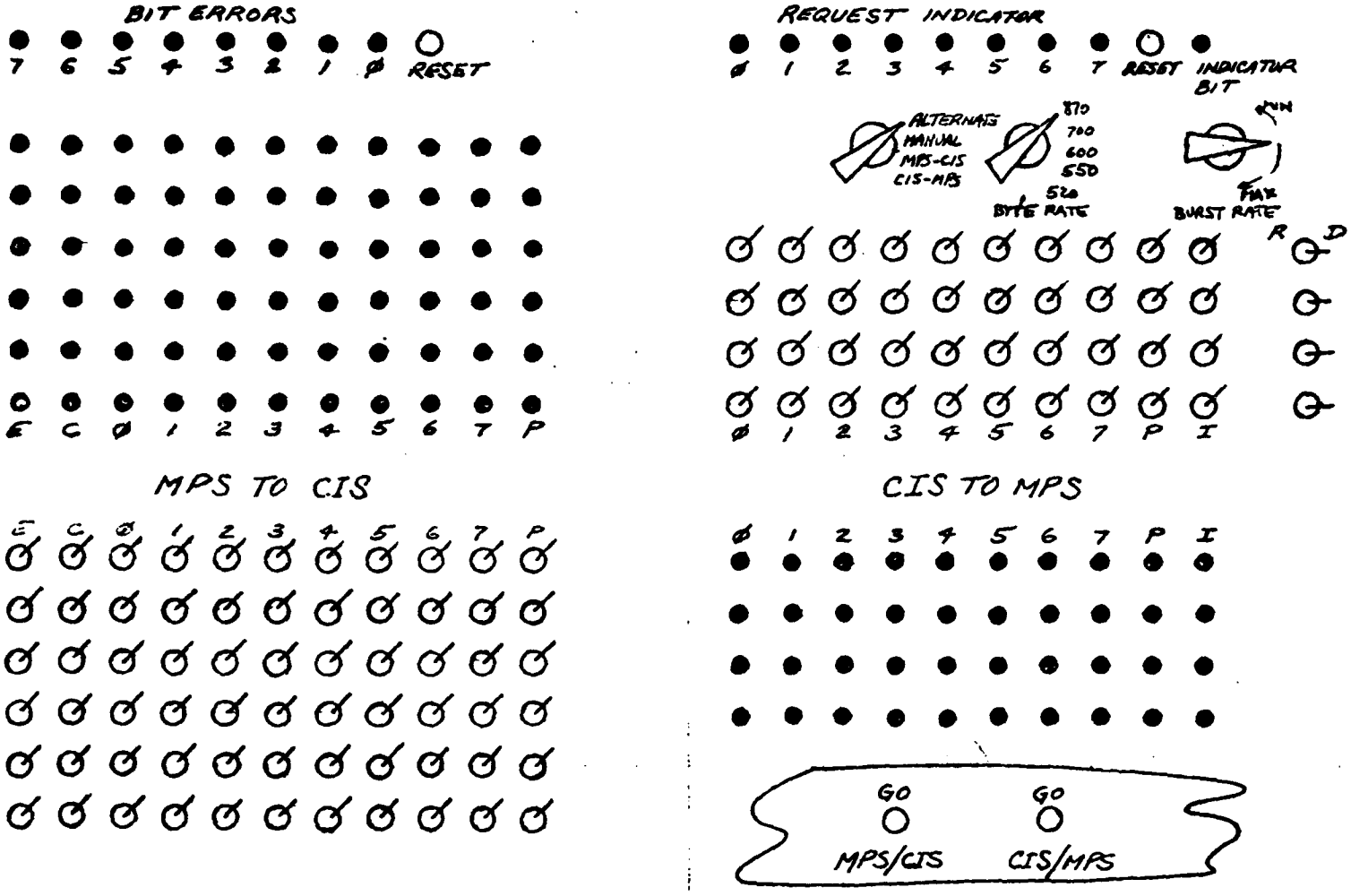


FIGURE B-8- IOX LINK TESTER PANEL

instruction code combinations can be sent and typical responses from CI returned. Delays can be measured each way and added together for substantiation of round-trip delay time. Alternatively, the ALTERNATE MODE could be used with the BURST RATE control adjusted to match the theoretical turn-around delay at the CI shelter end. Thus, the delay could be measured at the MP end alone.

For a logic diagram of the IOX Tester refer to the schematics in the rear pocket of this document.

The Loop Back Module depicted in Figures B-10 and B-11 can be attached to the IOX Tester in place of the UUT chassis. This permits the IOX Tester to directly receive its own transmission of data bytes and is used to establish Bit Error Rate performance in noisy environments. The box provides inversion and buffering of the IOX data bus, derives the expected data strobe pulse from the data bits, and provides the necessary time delay from the leading edge of the data to the leading edge of the strobe.

The part numbers and drawing numbers of the various pieces of IOX test equipment are as follows:

IOX Tester Assembly	01-1363974
Logic Diagram - IOX Tester	00-1363940
UUT Chassis Assembly	01-1363975
Logic Diagram - UUT Chassis	00-1363972
Loop Back Module Assembly	01-1363973
Logic Diagram - Loop Back Module	00-1363971

The UUT chassis provides a duplication of the IOX link and RCHYB card wiring as found in the deliverable LDFOCCS card nest.

RCHYB Card Testing

The IOX tester has been provided with the following interconnections from the RCHYB card socket for qualification testing. (Ref. Figure B-9).

Audio amplifier input (BP6)

Audio amplifier output (BP8)

Detector input (BP3)

Detector output (BP5)

Enable toggle

Crystal oscillator output (BP1/BP2)

The AUDIO INPUT will be driven with 600ohm unbalanced audio generator and the AUDIO OUTPUT will be examined with oscilloscope to ascertain design value of gain, lack of any significant distortion, and an indication that the amplifier can be disabled by the operation of the ENABLE TOGGLE. The DETECTOR INPUT will be driven with 600 ohm balanced audio generator and the DETECTOR OUTPUT will be examined by oscilloscope for an indication that the logic level switches at the design threshold. The OSCILLATOR OUTPUT will be examined for waveshape, and frequency measured by counter.

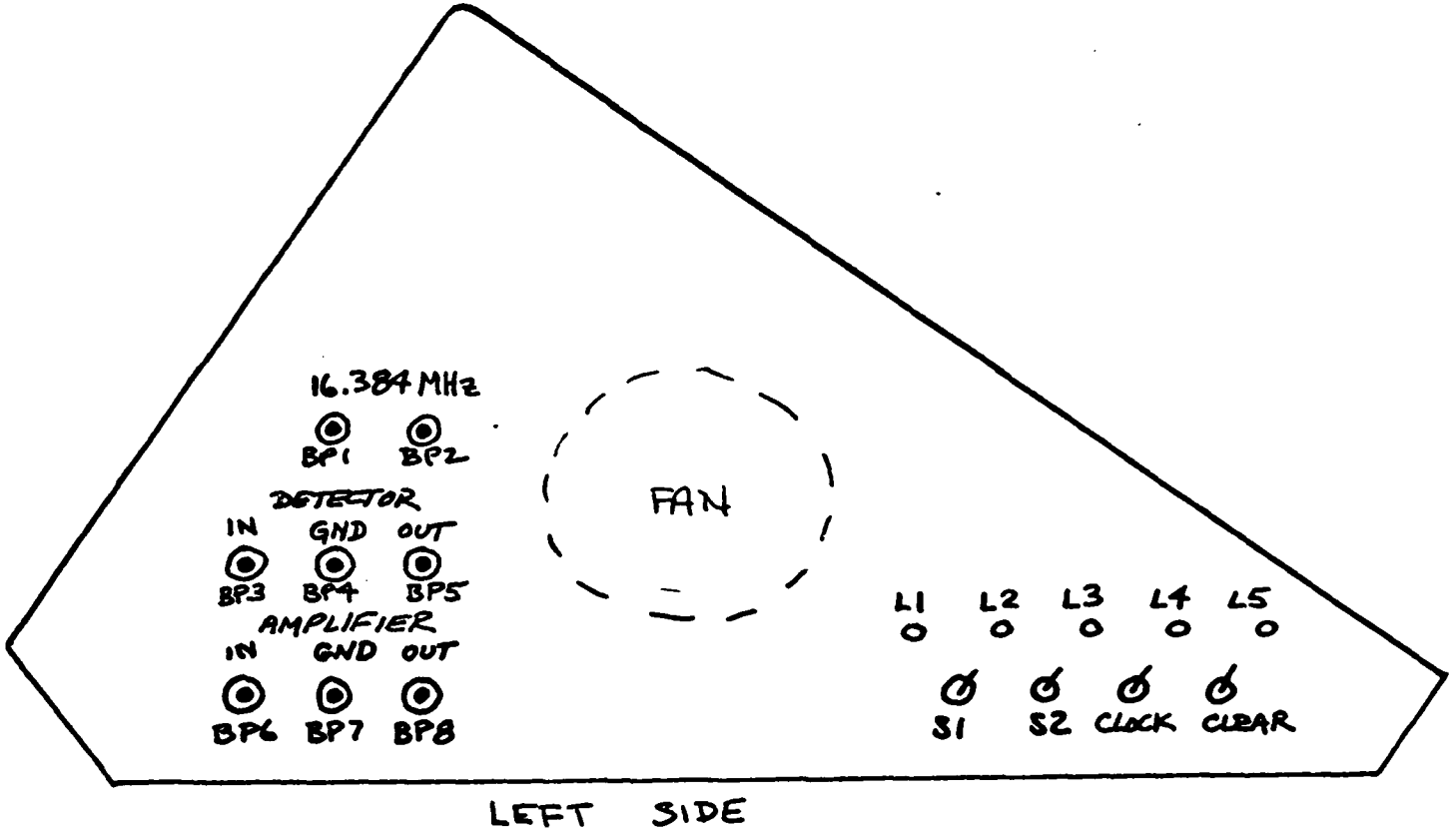


FIGURE B-9 - 10X TESTER SIDE PANEL

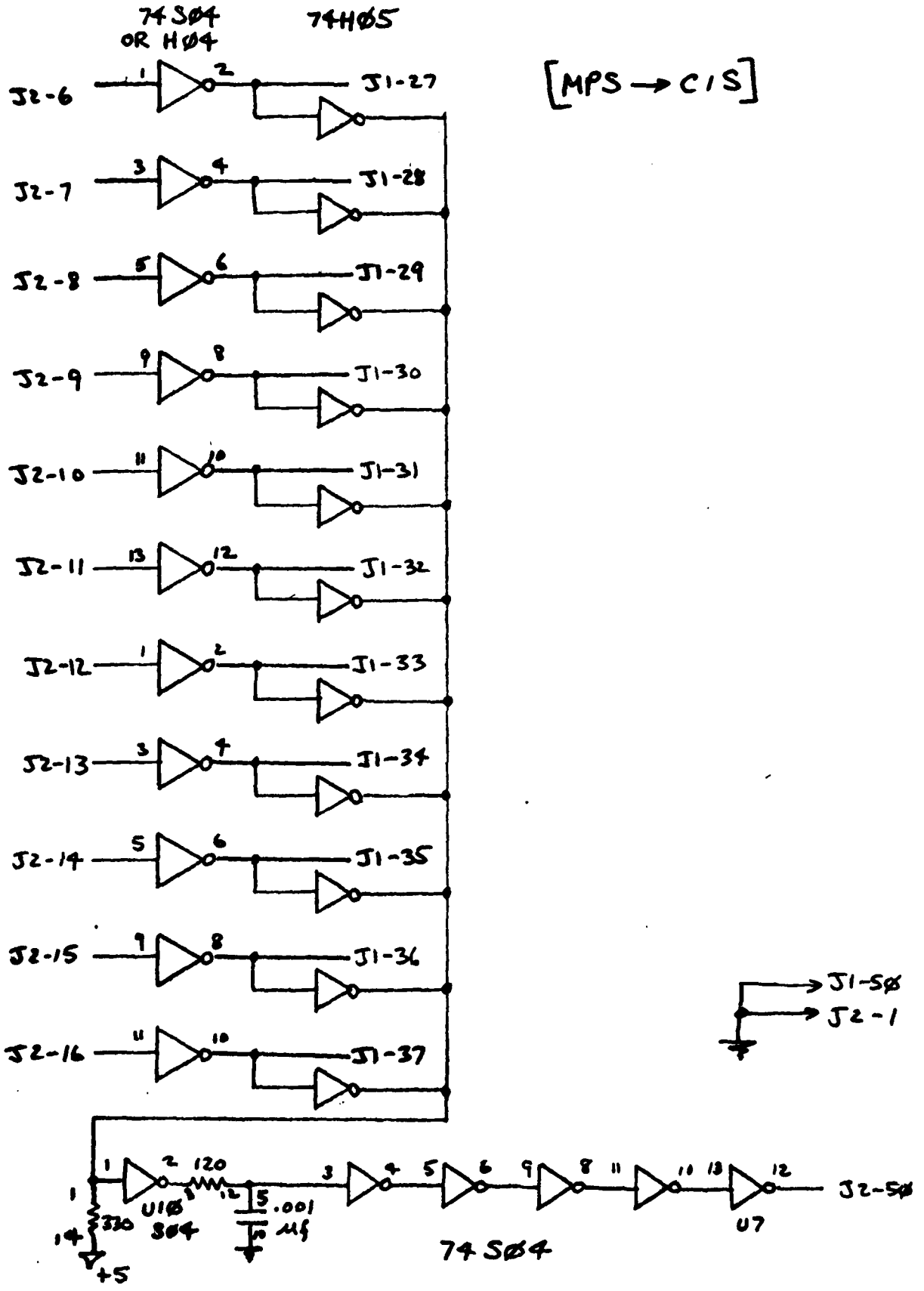


FIGURE B-10 - TESTER CAL. BOX

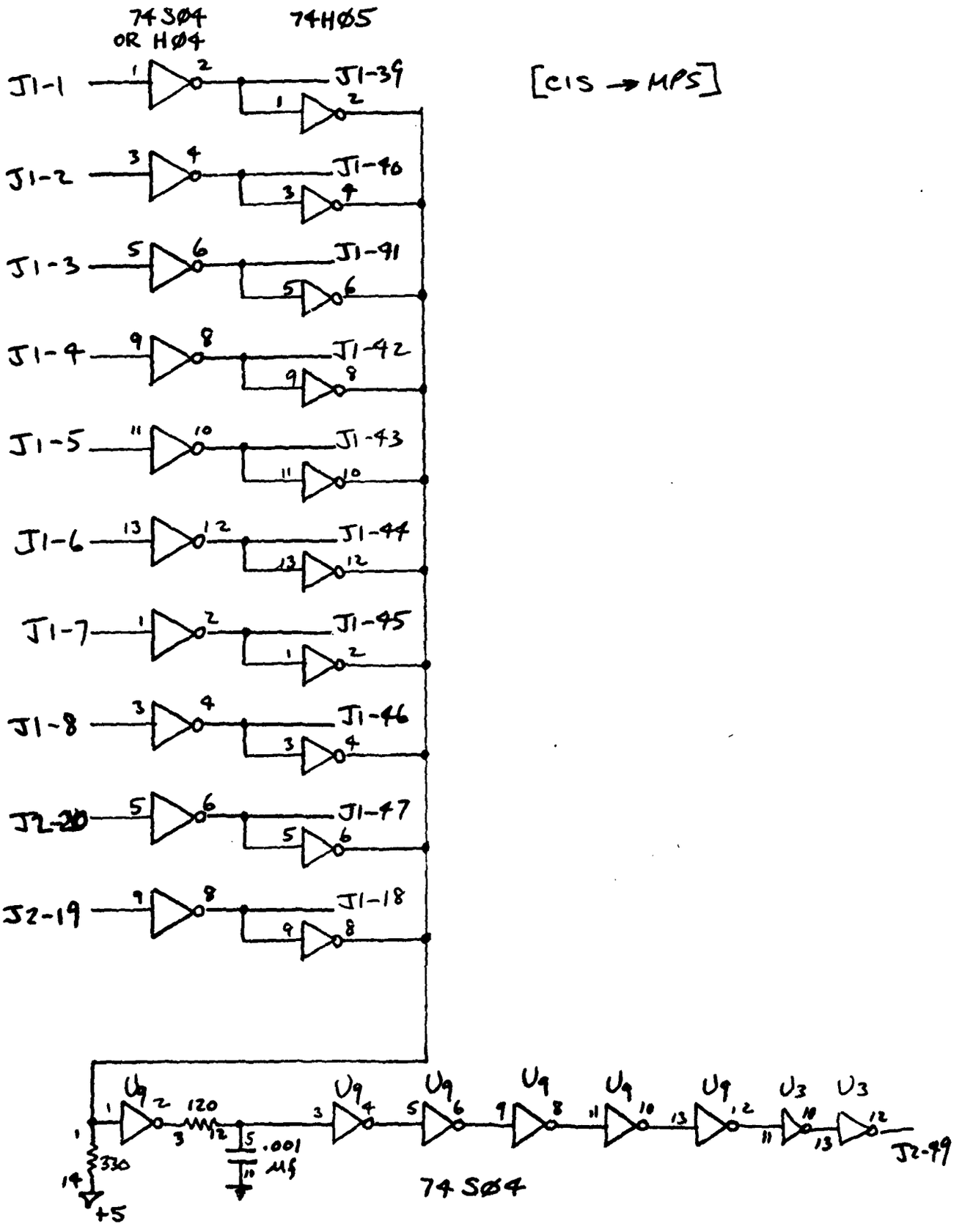


FIGURE B-11 - TESTER CAL. BOX

IOX Tester and UUT Chassis Description

The IOX Tester and UUT chassis hardware has been designed fabricated and checked out, and is currently in use for design verification, with an intended future use in design qualification. The equipment is oriented around the new design card types for LDFOCCS, namely, the IOX link cards, Optical Modem card and RCHYB card. The test chassis accomodates two IOX-T, two IOX-R and one Optical Modem card to form one complete three-fiber, IOX end-to-end link. One socket accepts the RCHYB card for qualification of the intercom amplifier/direction control circuit two crystal oscillators, and the TGM sync logic for the C&S subsystem. In conjunction with the test chassis, a set of card extenders will be used to make the conversion between the present breadboard card connectors at production card testing and qualification testing times. Other connectors on the test chassis accept cable cards for interconnection to the IOX link tester.

The block diagram of the IOX Link Tester is shown in figure B-1. The desired test pattern is set up on the bank of 6X11 switches (fig. B-2) representing data from the CPU end of the link. The 11 bits represent the parallel byte from the processor, and the 6 bits represent the maximum number of bytes in a single transmission from the CPU in the MS shelter to peripherals in the CI shelter. Each byte of switches is gated in time sequence to the lines in the cable leading to the test chassis IOX-T card inputs. At the IOX-R receiving end of the test chassis the parallel outputs presented via cable to the tester are accumulated in a bank of shift registers having LED indicators (fig. B-3).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